FIG. 1

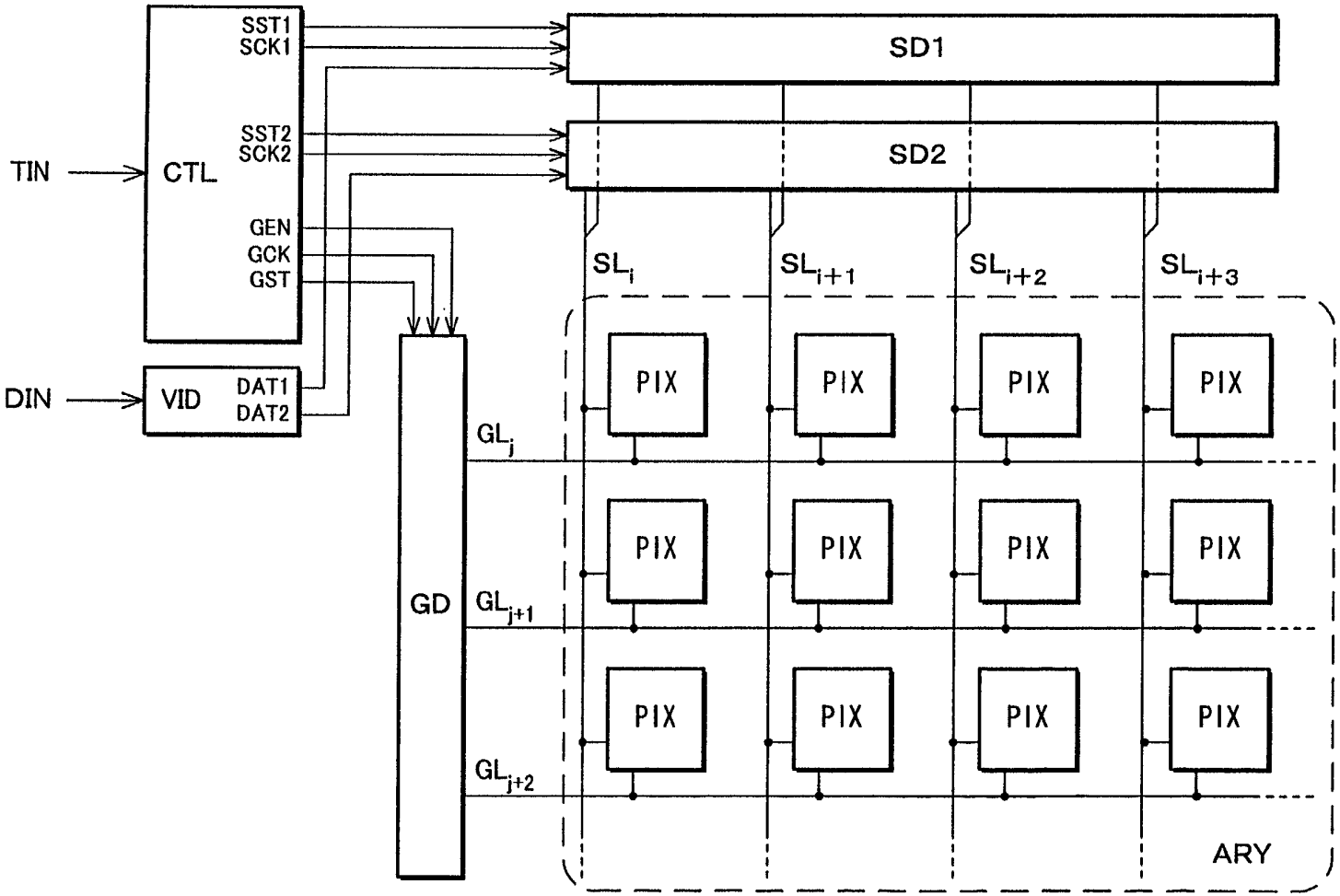

SST1
SCK1
SST2
SCK2
GEN
GCK
GST
CTL
TIN
DIN
VID
DAT1
DAT2
SD1
SD2
GD
SL_i
SL_{i+1}
SL_{i+2}
SL_{i+3}
GL_j
GL_{j+1}
GL_{j+2}
PIX
ARY

FIG. 2

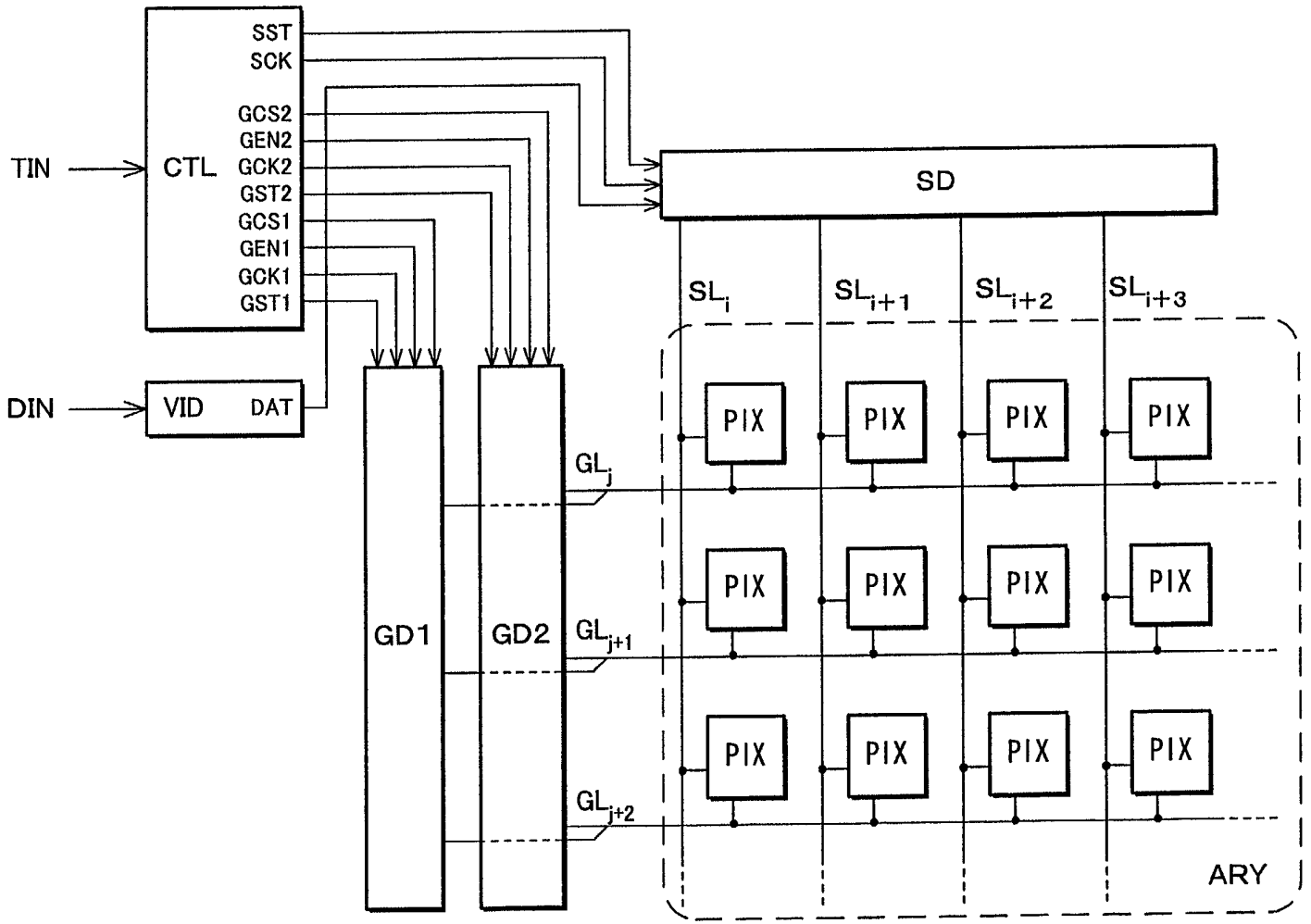

SST
SCK
GCS2
GEN2
GCK2
GST2
GCS1
GEN1
GCK1
GST1
TIN
CTL
DIN
VID
DAT
SD
SL_i
SL_i+1
SL_i+2
SL_i+3
PIX
GL_j
GL_j+1
GL_j+2
GD1
GD2
ARY

FIG. 3

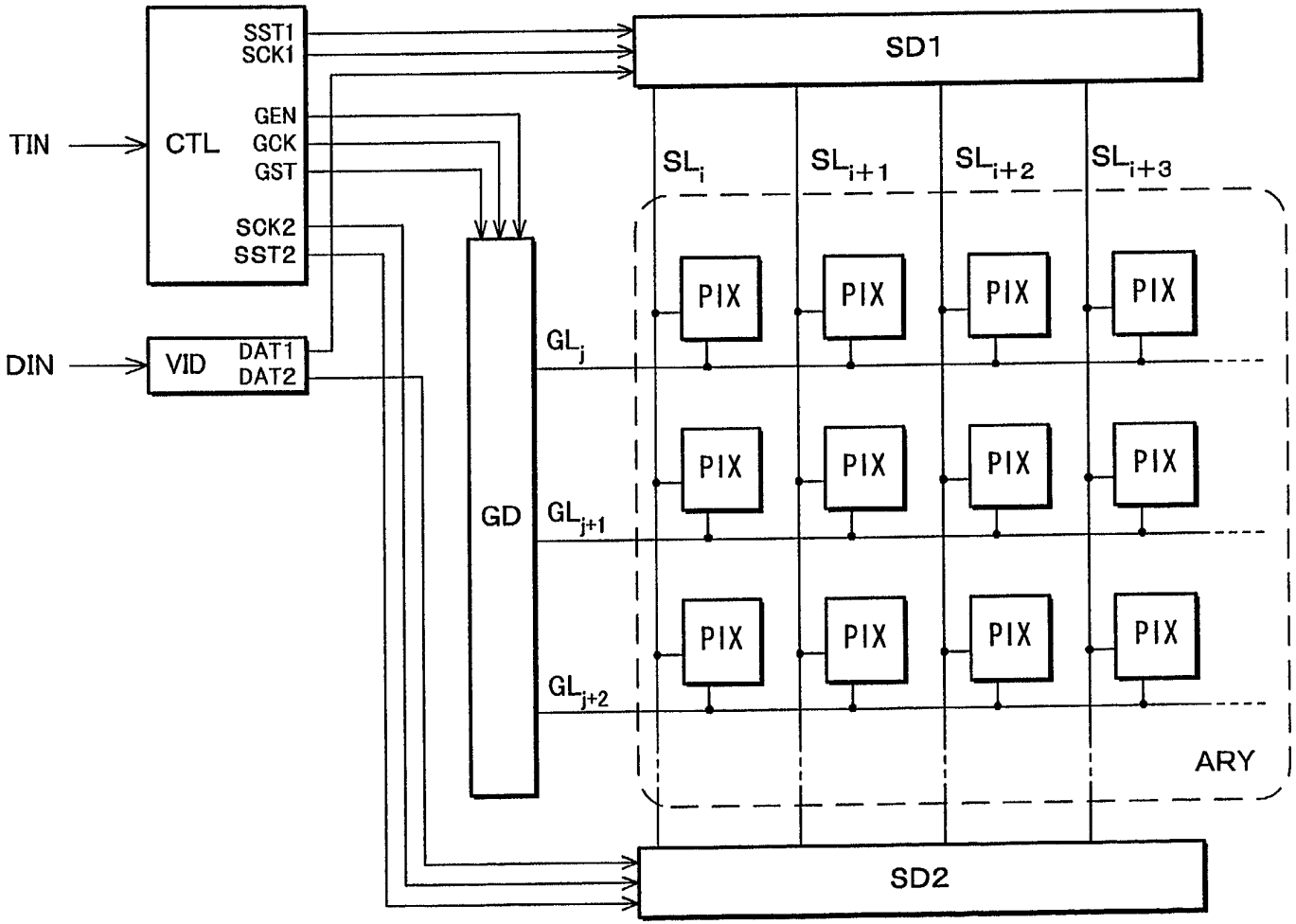
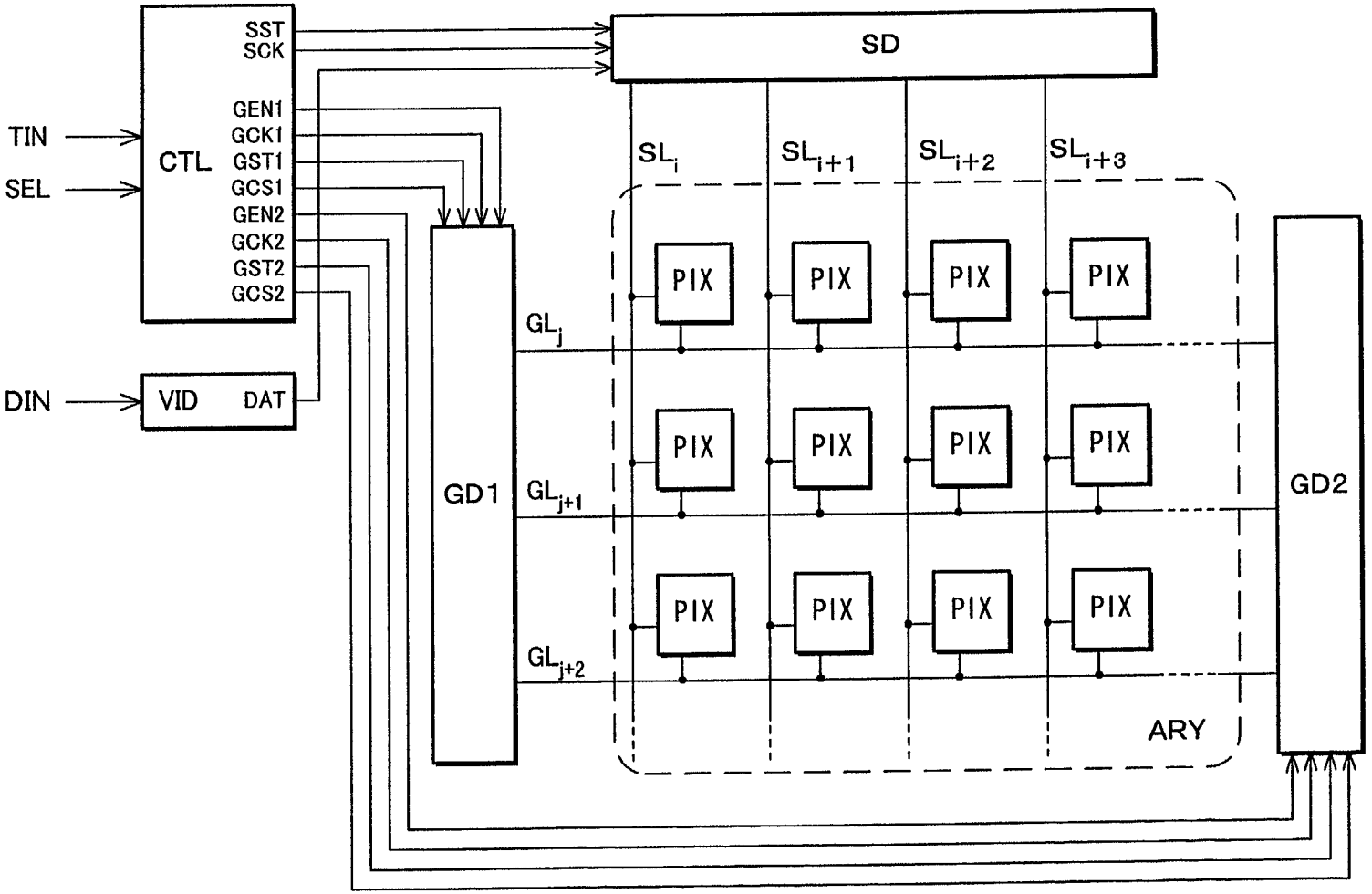

SST1
SCK1
GEN
GCK
GST
SCK2
SST2
CTL
TIN
DIN
VID
DAT1
DAT2
SD1
SD2
GD
SL_i
SL_{i+1}
SL_{i+2}
SL_{i+3}
GL_j
GL_{j+1}
GL_{j+2}
PIX
ARY

FIG. 4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SCK
SD
GEN1
GCK1
GST1
GCS1
GEN2
GCK2
GST2
GCS2
TIN
SEL
CTL
DIN
VID
DAT
SL_i
SL_i+1
SL_i+2
SL_i+3
GD1
GL_j
GL_j+1
GL_j+2
PIX
GD2
ARY

FIG. 5

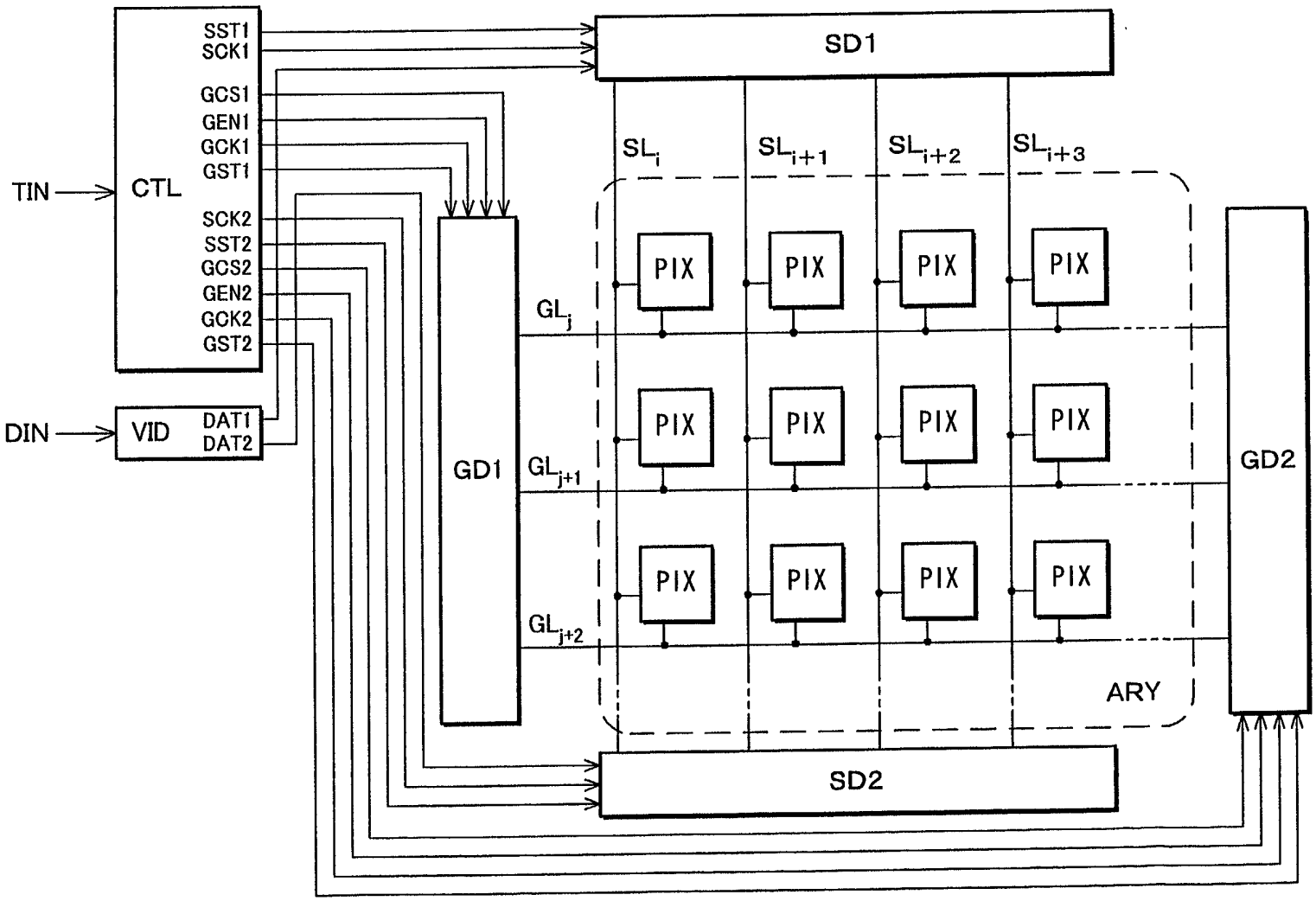
SST1
SCK1
GCS1
GEN1
GCK1
GST1
SCK2
SST2
GCS2
GEN2
GCK2
GST2
TIN
CTL
DIN
VID
DAT1
DAT2
SD1
SD2
GD1
GD2
SL_i
SL_i+1
SL_i+2
SL_i+3
GL_j
GL_j+1
GL_j+2
PIX
ARY

FIG. 6

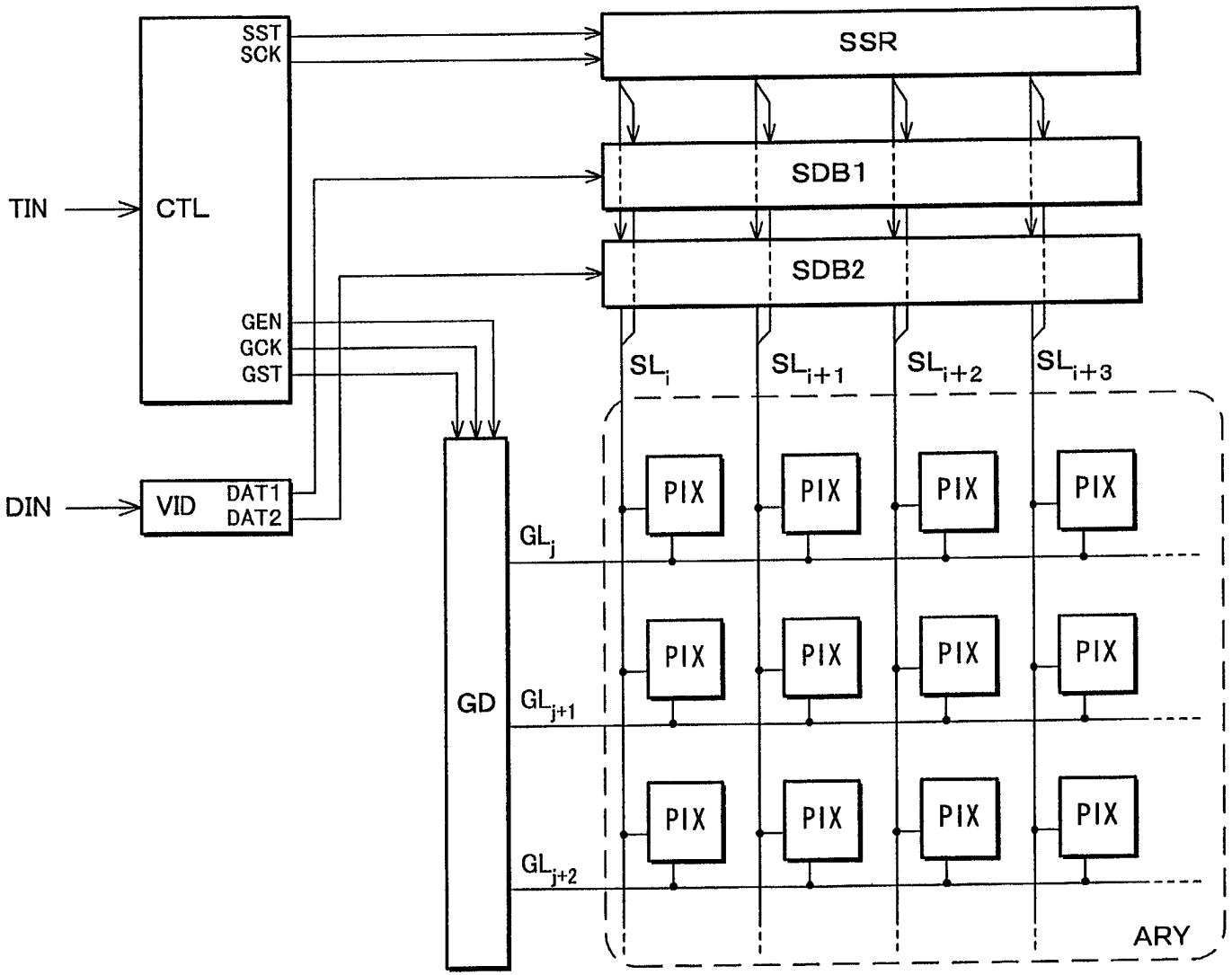
SST
SCK
SSR
SDB1
SDB2
TIN
CTL
GEN
GCK
GST
SL_i
SL_i+1
SL_i+2
SL_i+3
DIN
VID
DAT1
DAT2
GD
GL_j
GL_j+1
GL_j+2
PIX
ARY

FIG. 7

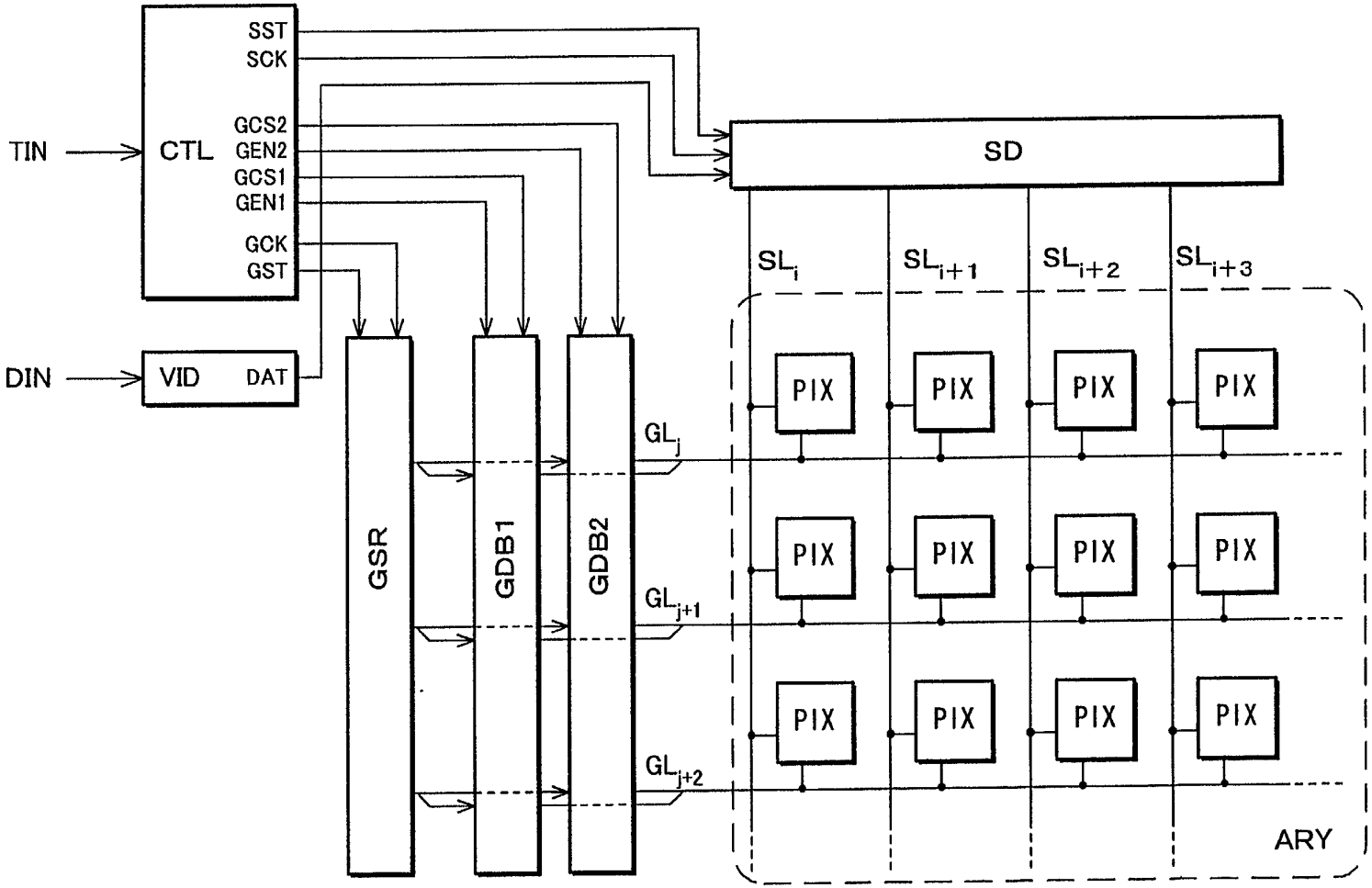
SST
SCK
GCS2
GEN2
GCS1
GEN1
GCK
GST
TIN
CTL
DIN
VID
DAT
SD
SL_i
SL_{i+1}
SL_{i+2}
SL_{i+3}
GSR
GDB1
GDB2
GL_j
GL_{j+1}
GL_{j+2}
PIX
ARY

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FIG. 8

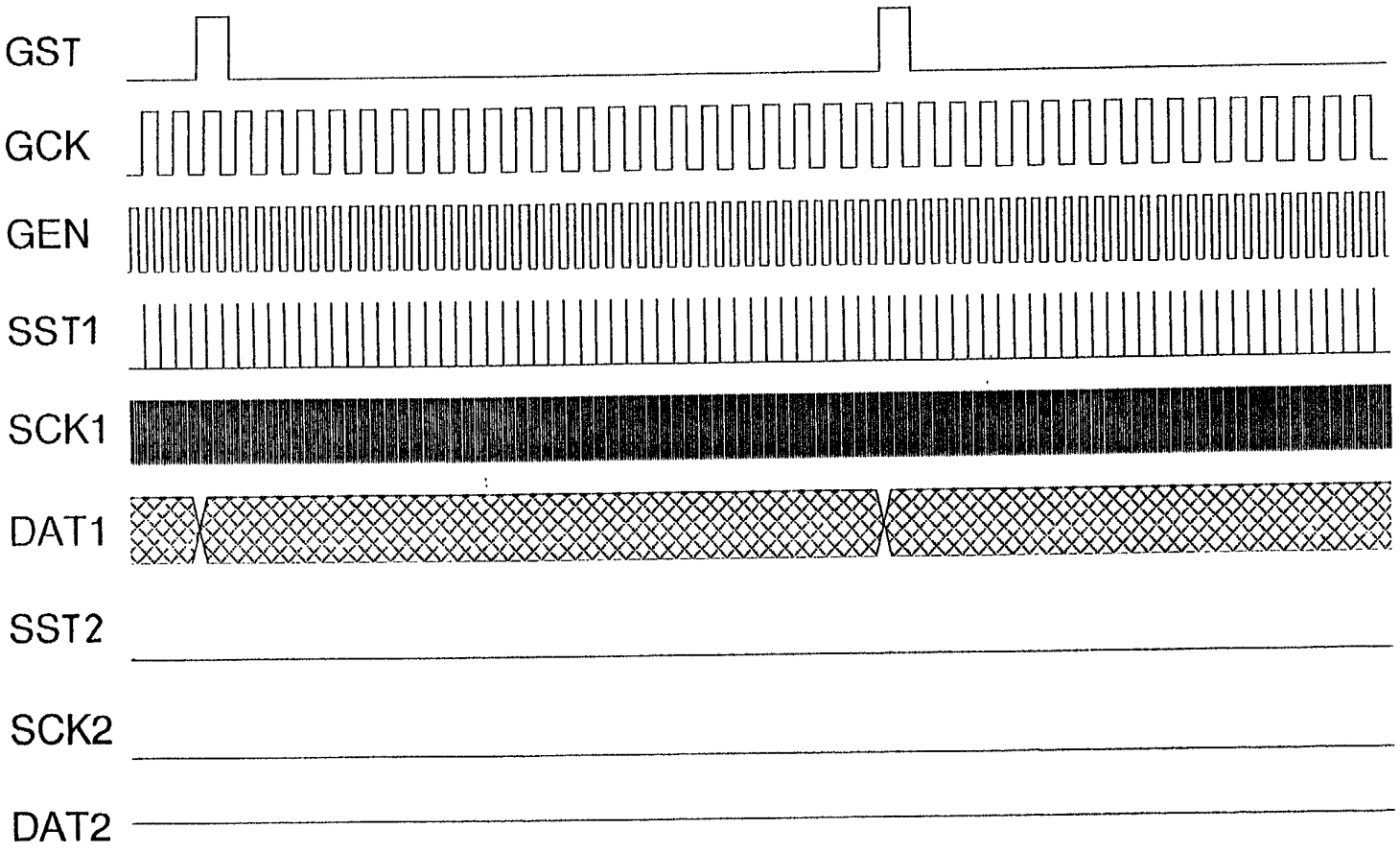

FIG. 9

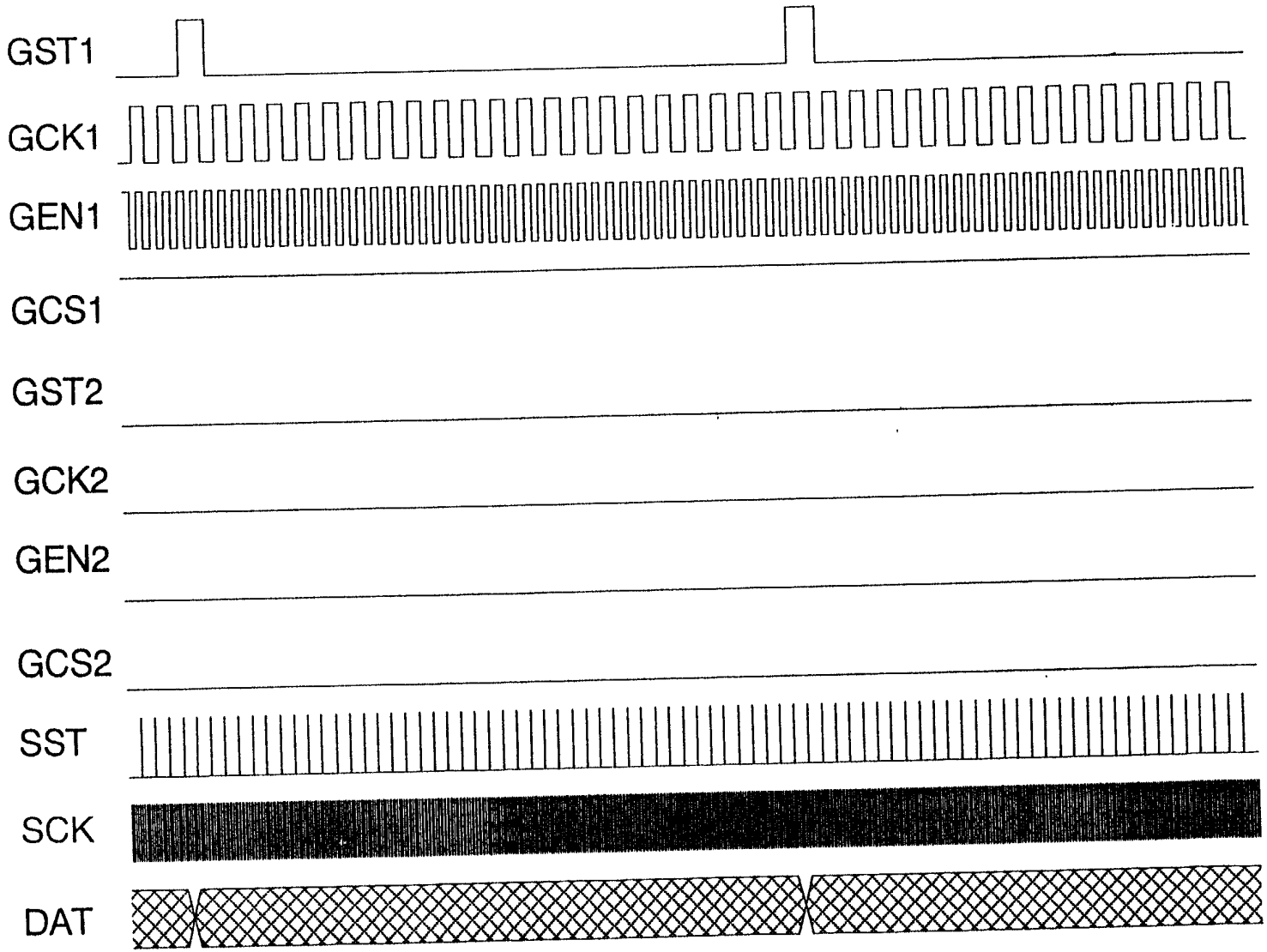

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FIG. 10

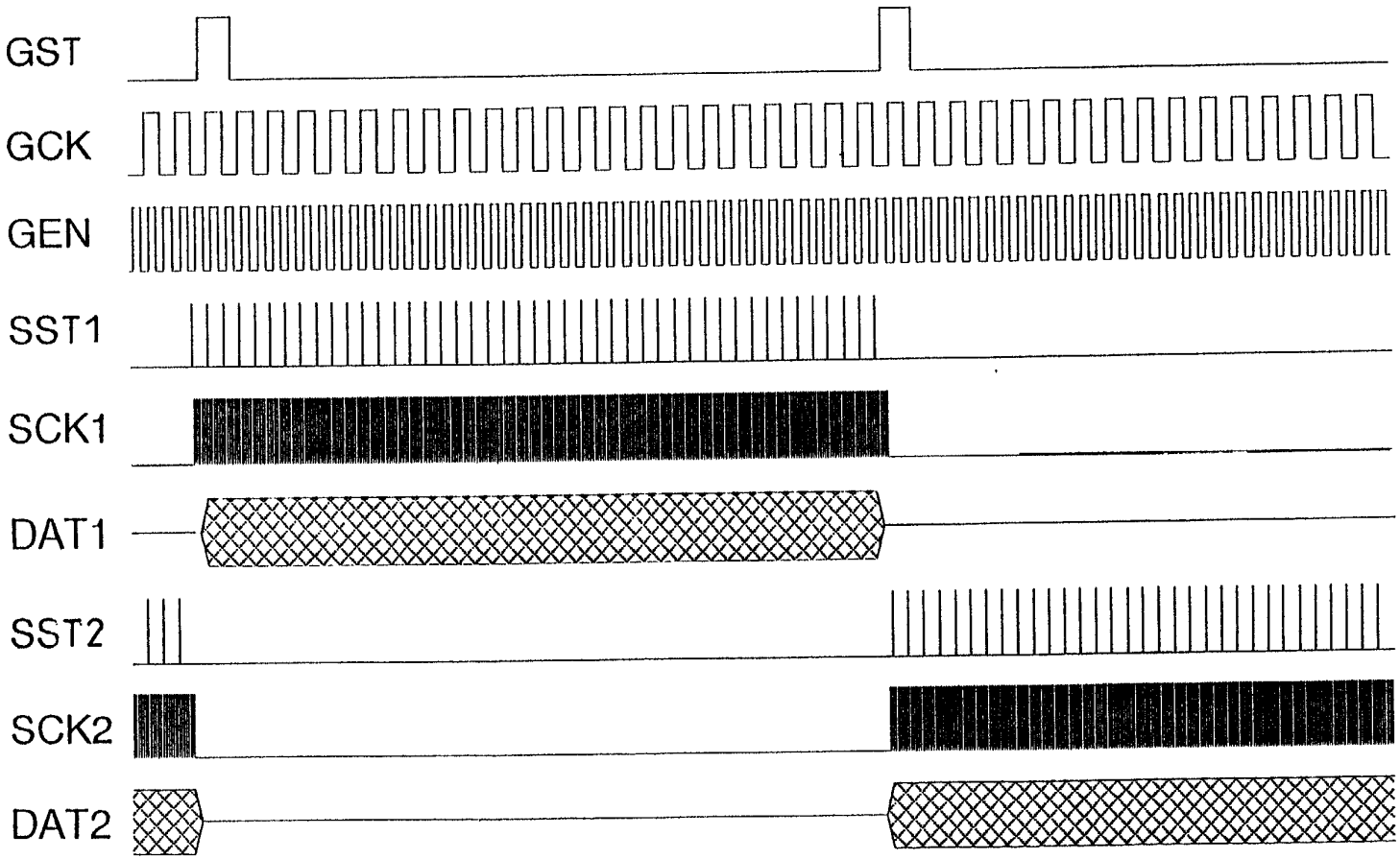

FIG. 11

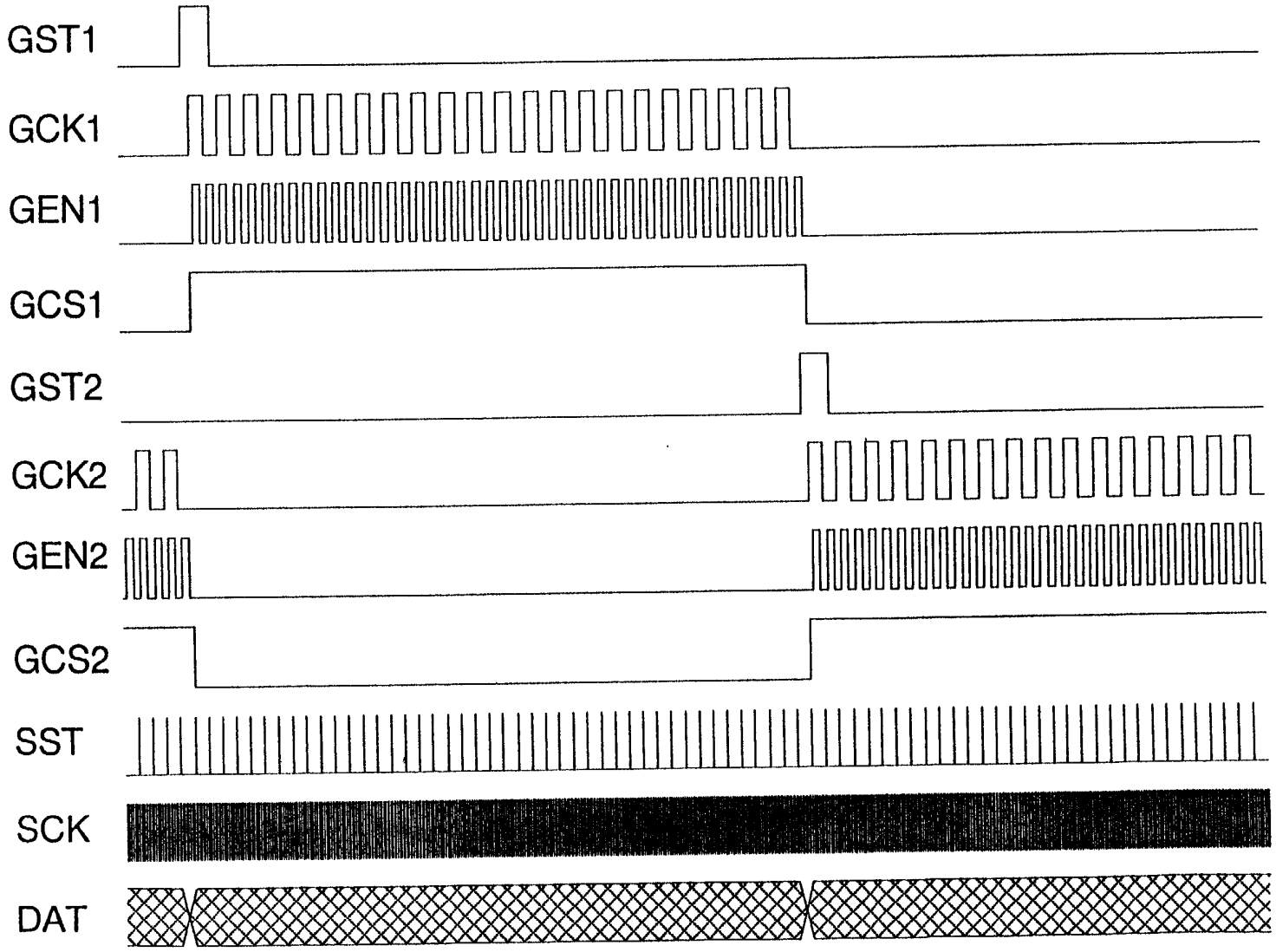

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FIG. 12

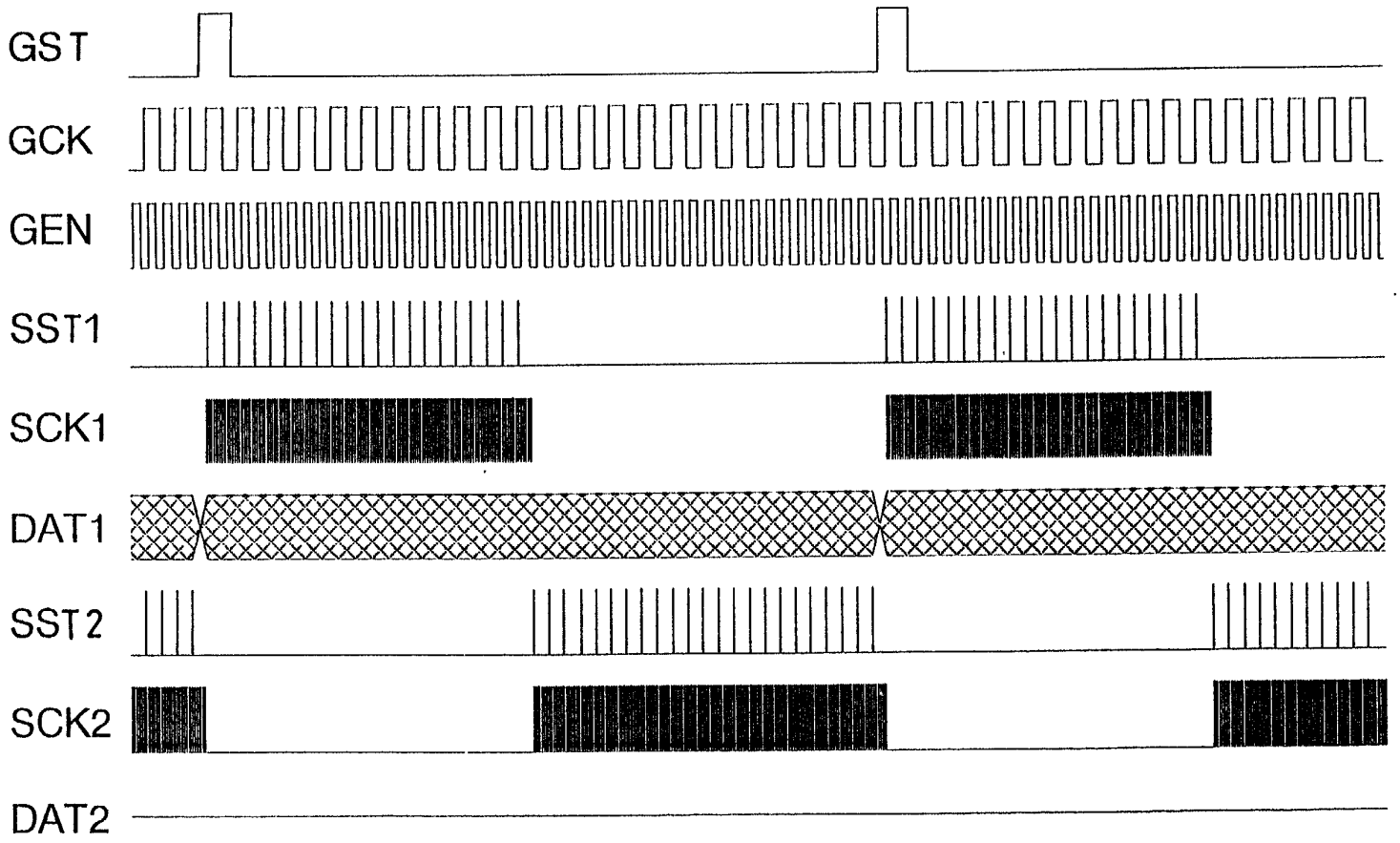

FIG.13

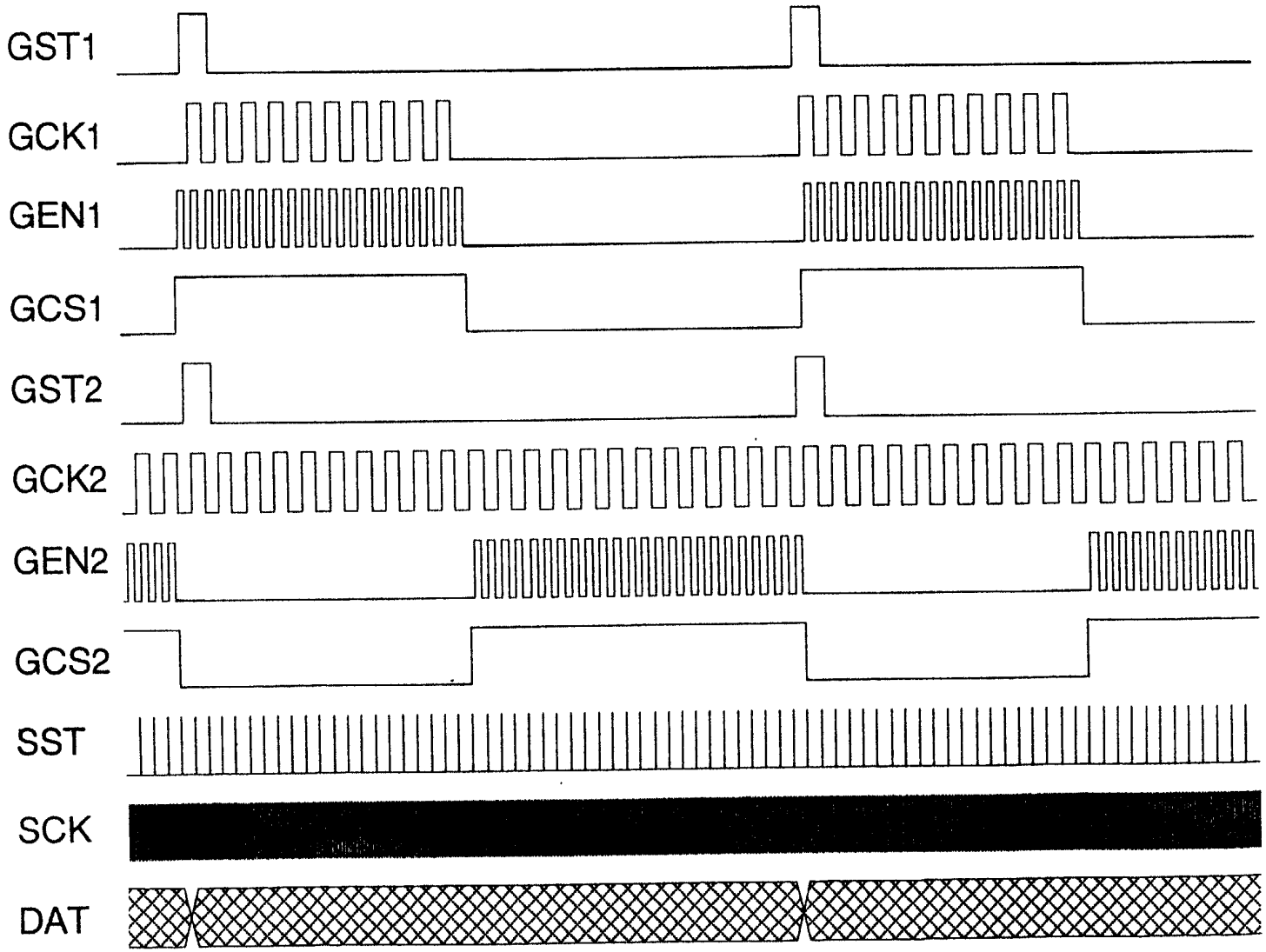

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FIG. 14(a)

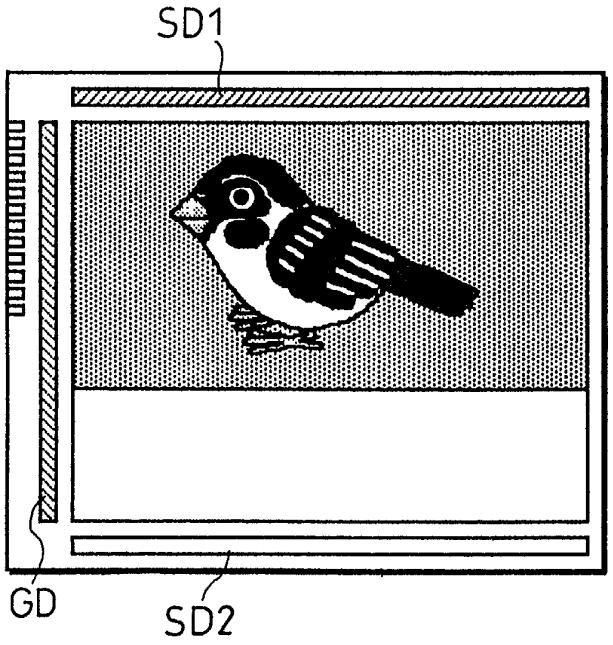
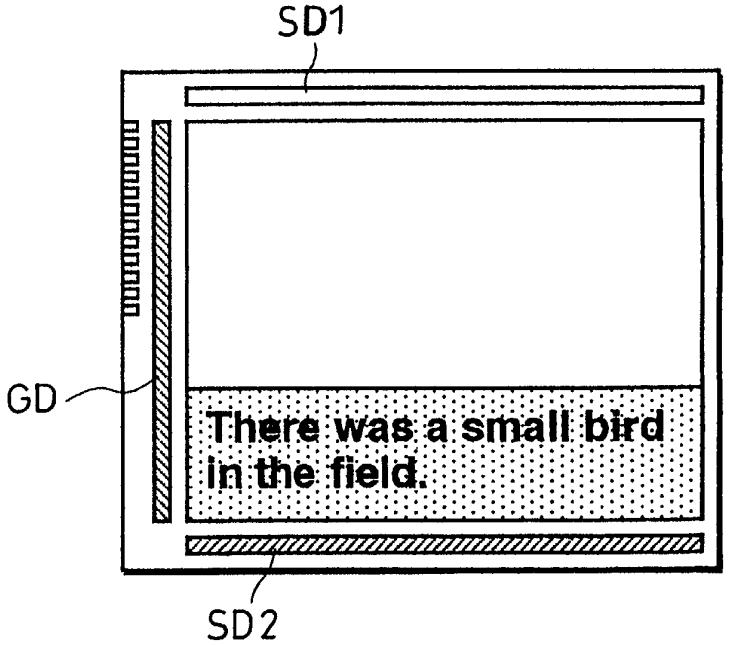


FIG. 14(b)



JP06050588B2

FIG. 15(a)

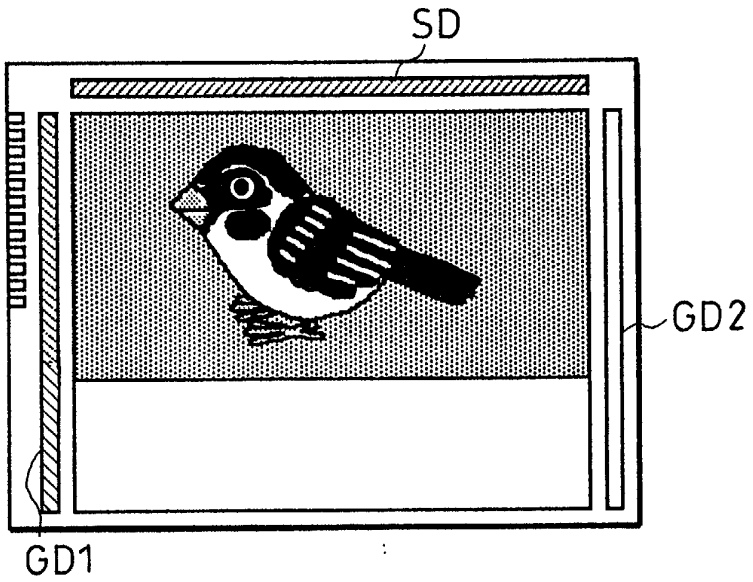


FIG. 15(b)

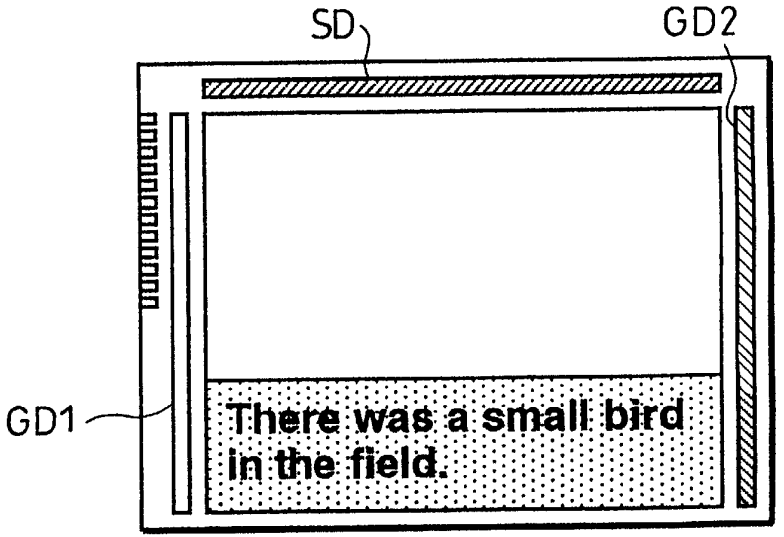


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FIG.16

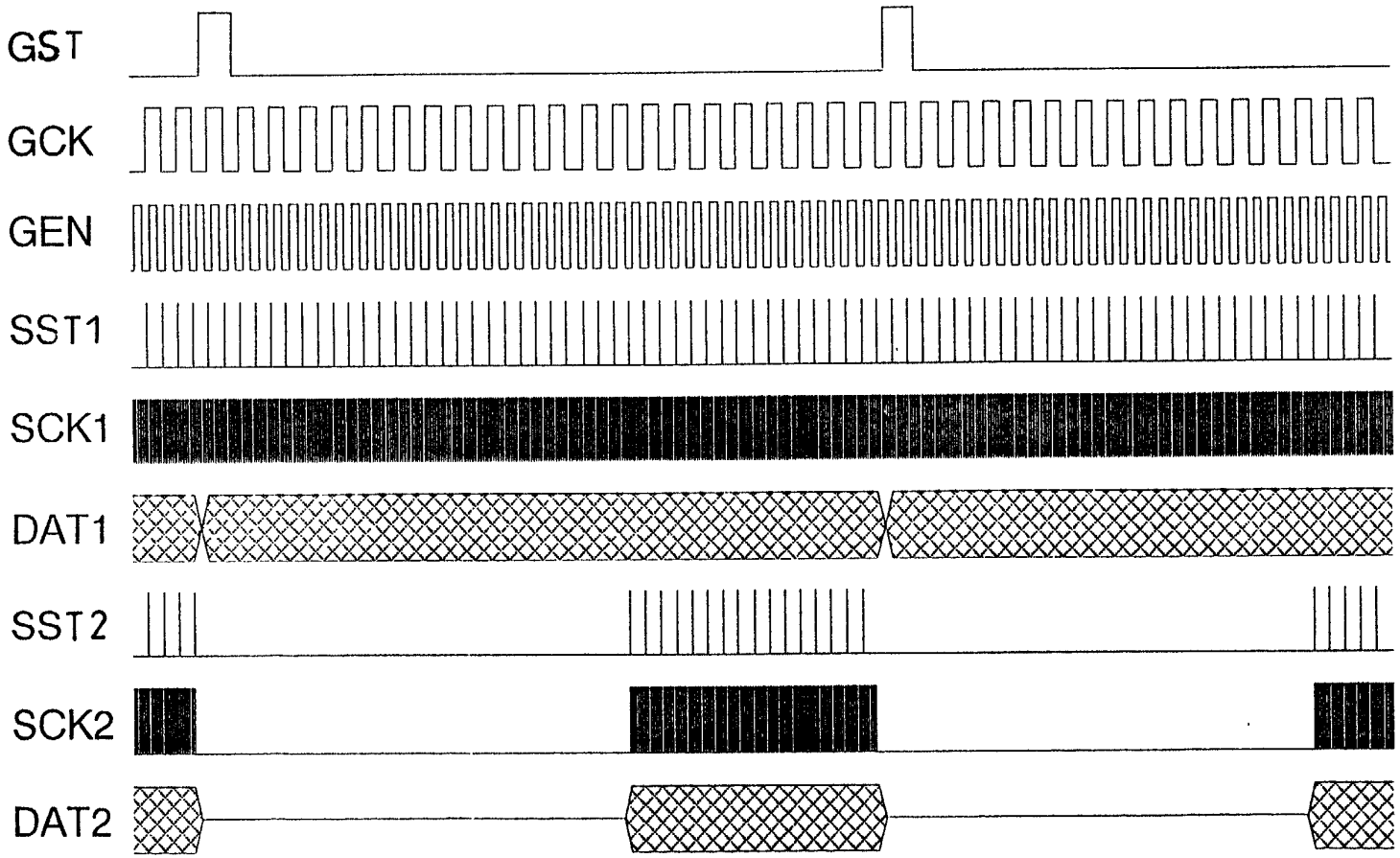

FIG.17(a)

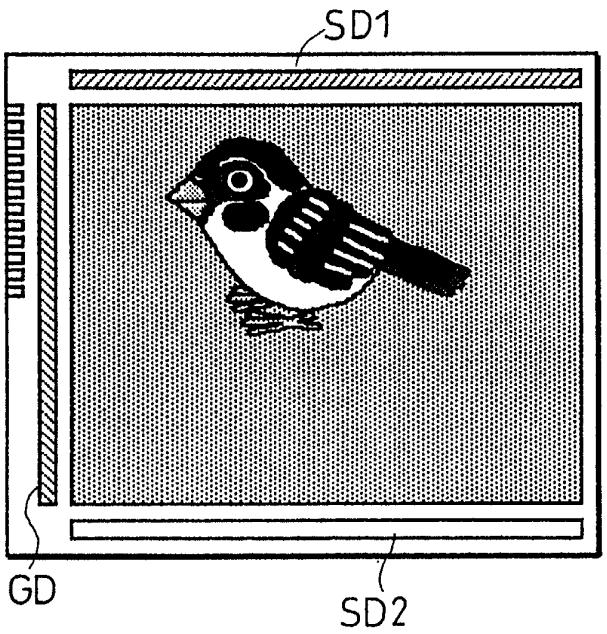

FIG.17(b)

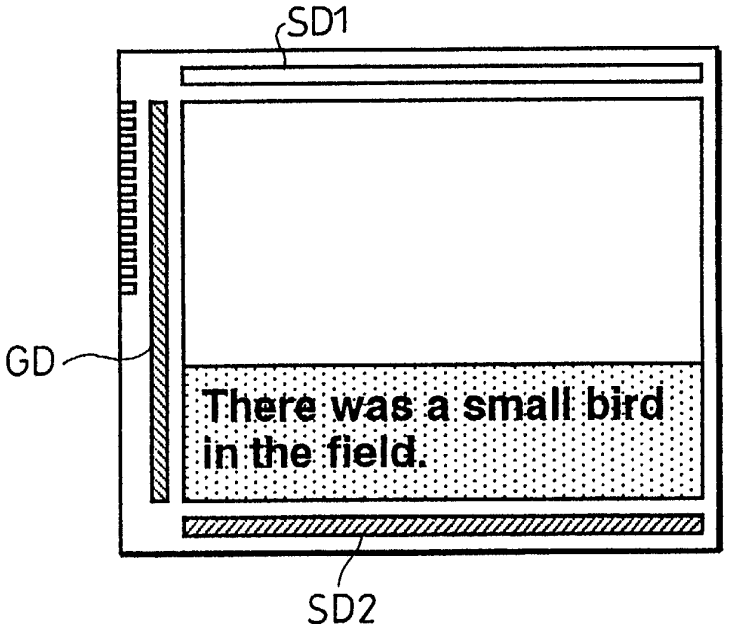

FIG. 18

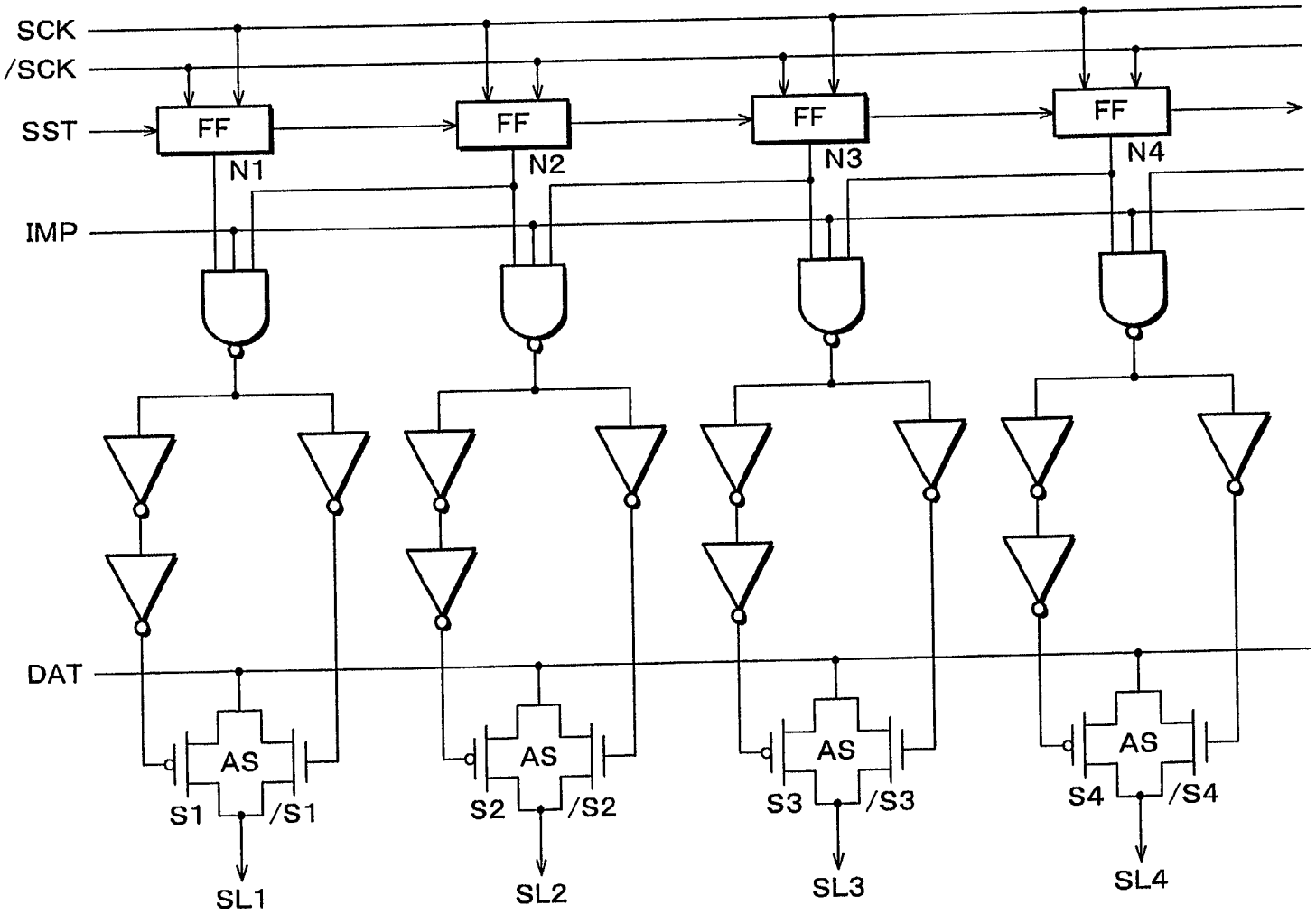
SCK
/SCK
SST
IMP
DAT
FF
N1
FF
N2
FF
N3
FF
N4
AS
S1
/S1
SL1
AS
S2
/S2
SL2
AS
S3
/S3
SL3
AS
S4
/S4
SL4

FIG. 19

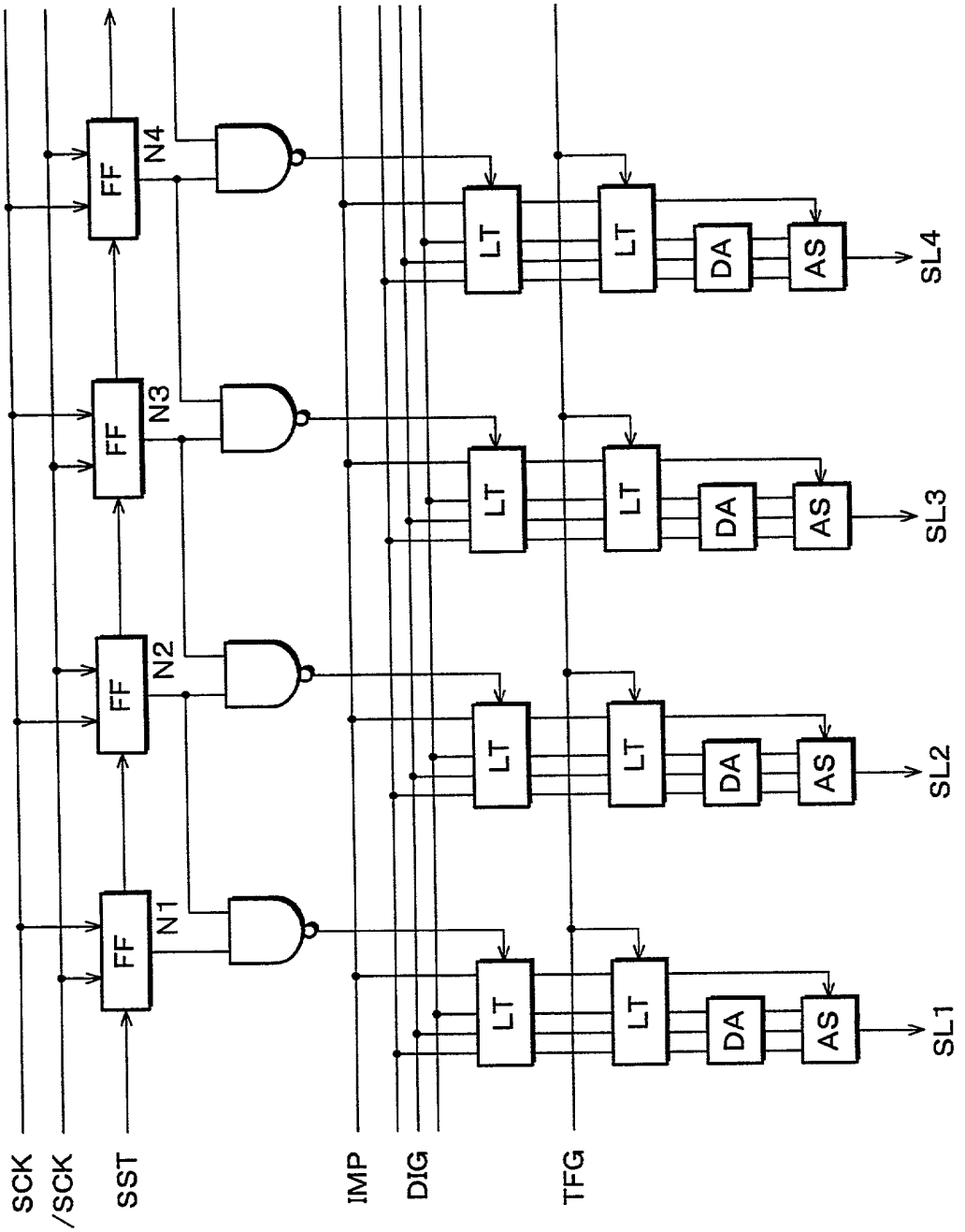

FIG. 20

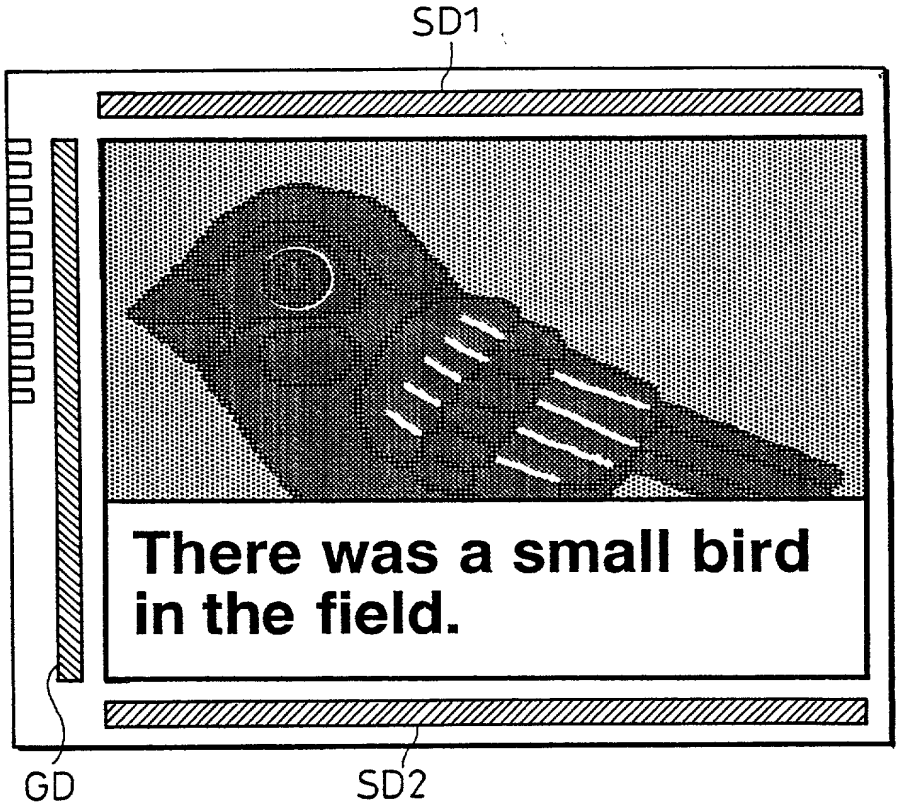

FIG. 21

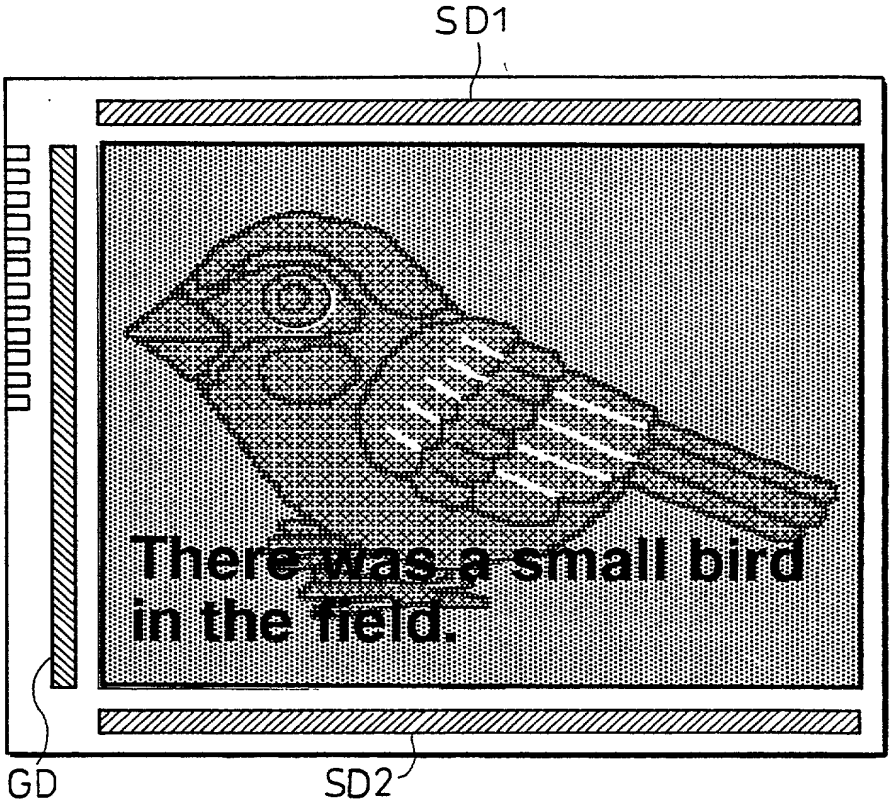

FIG. 22

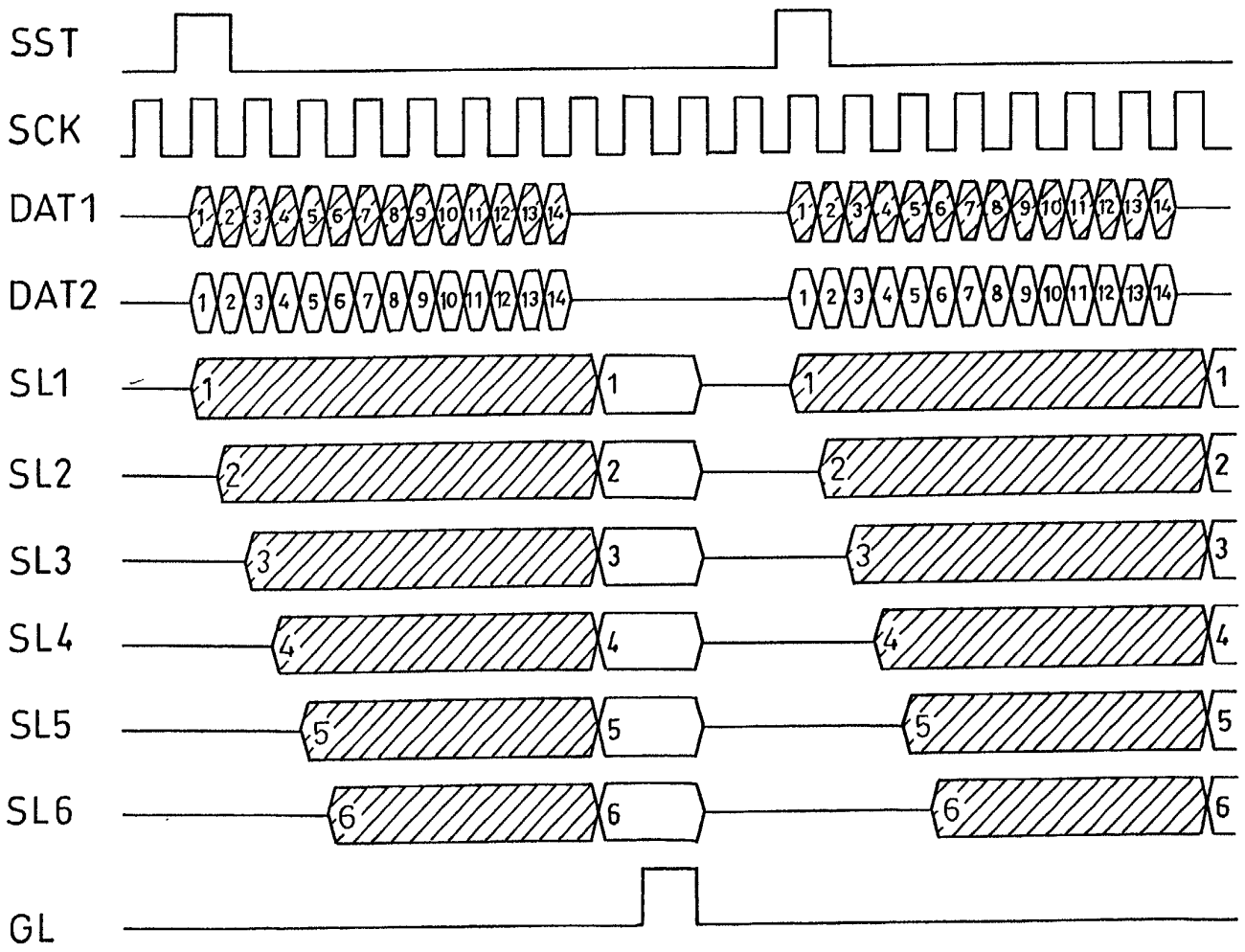

FIG. 23

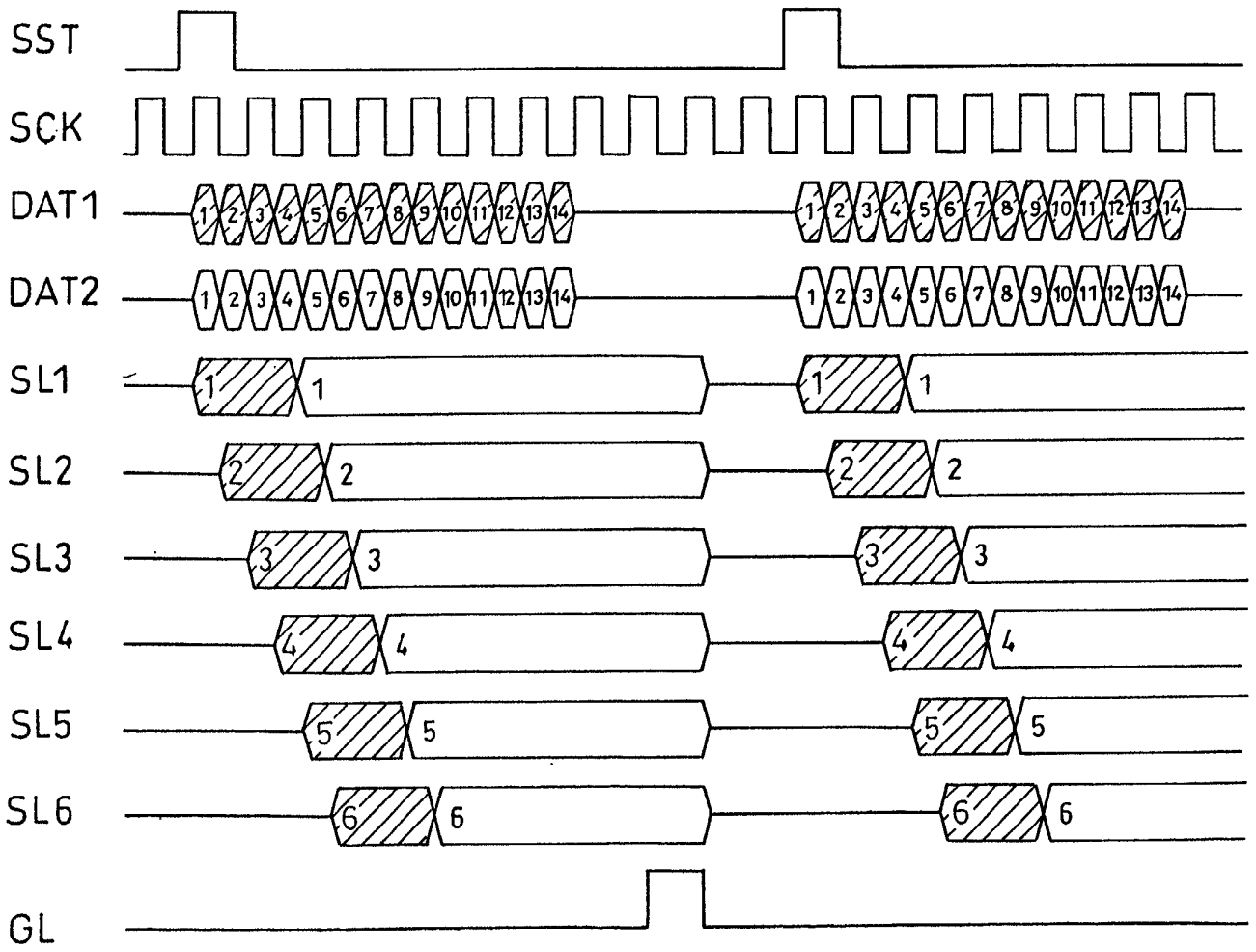

FIG. 24

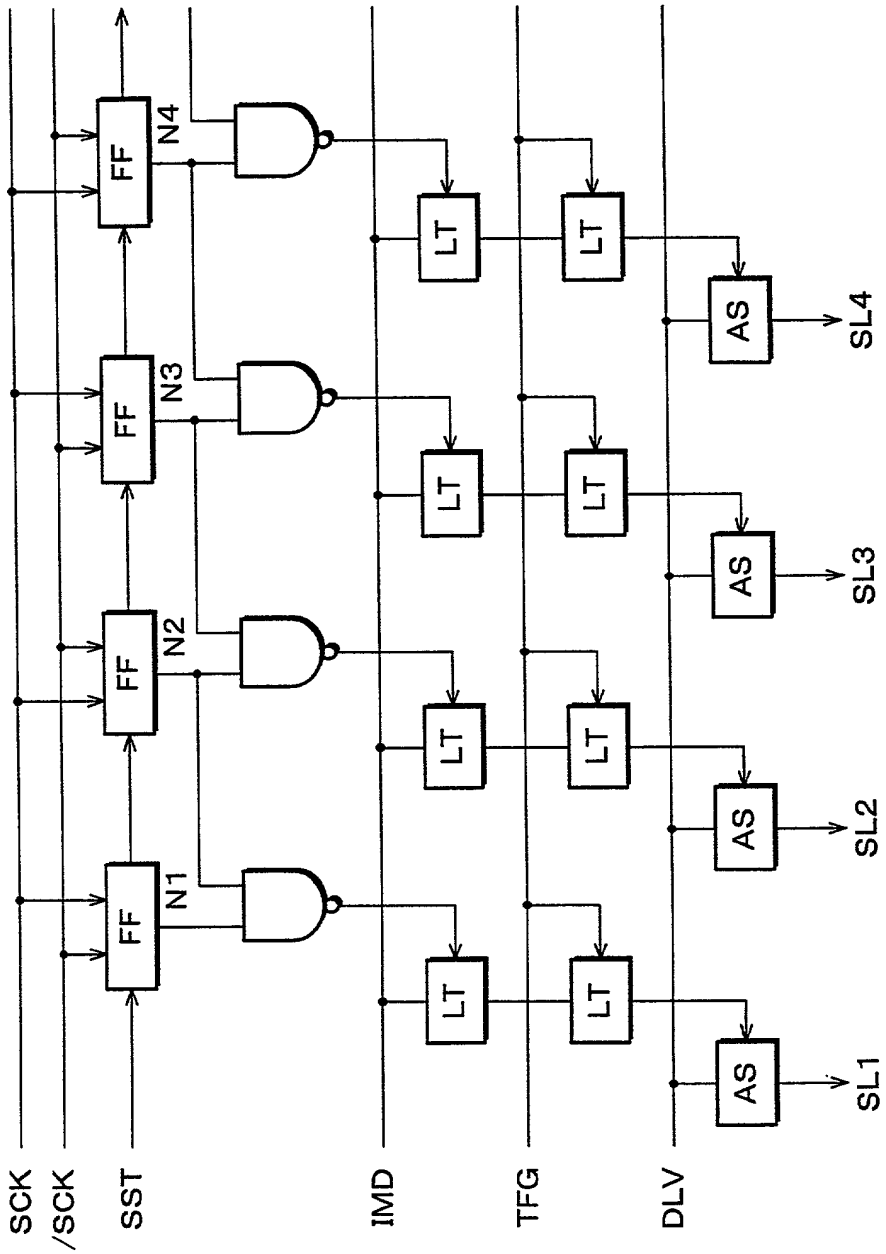

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FIG. 25

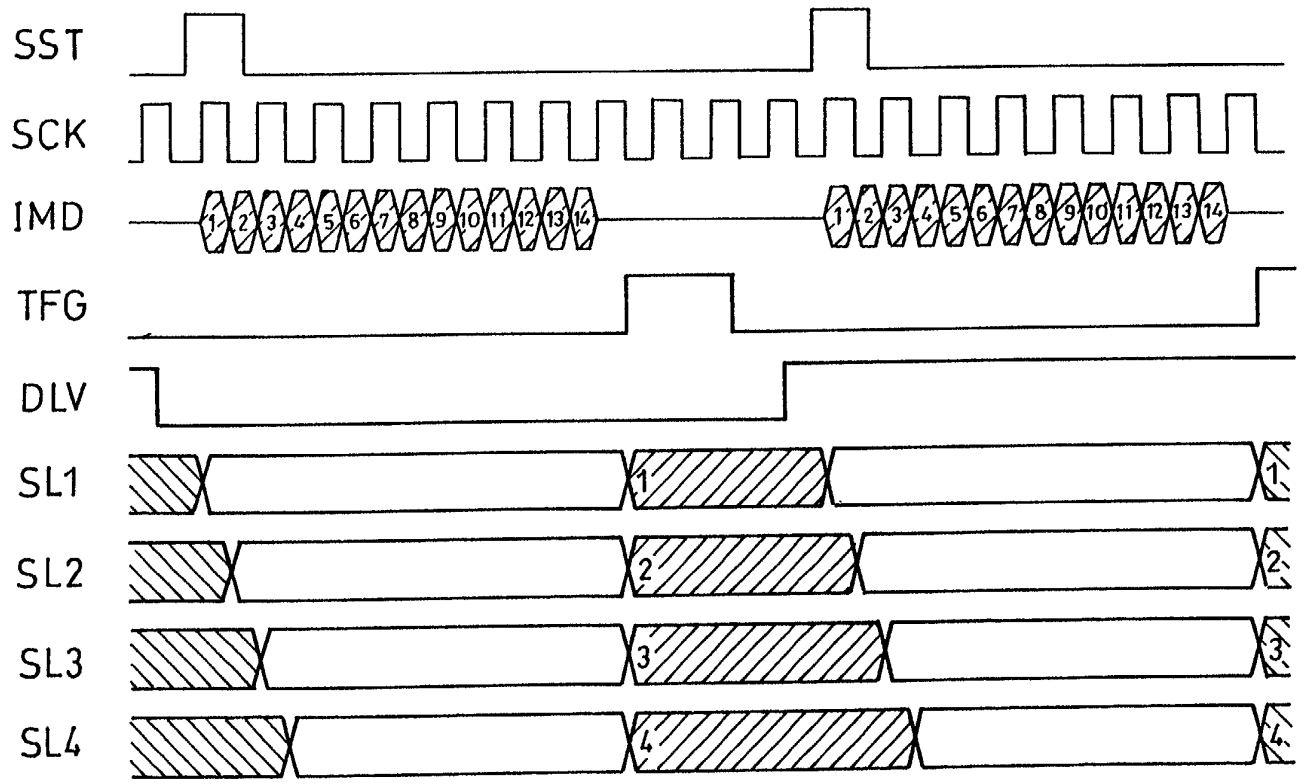

FIG. 26

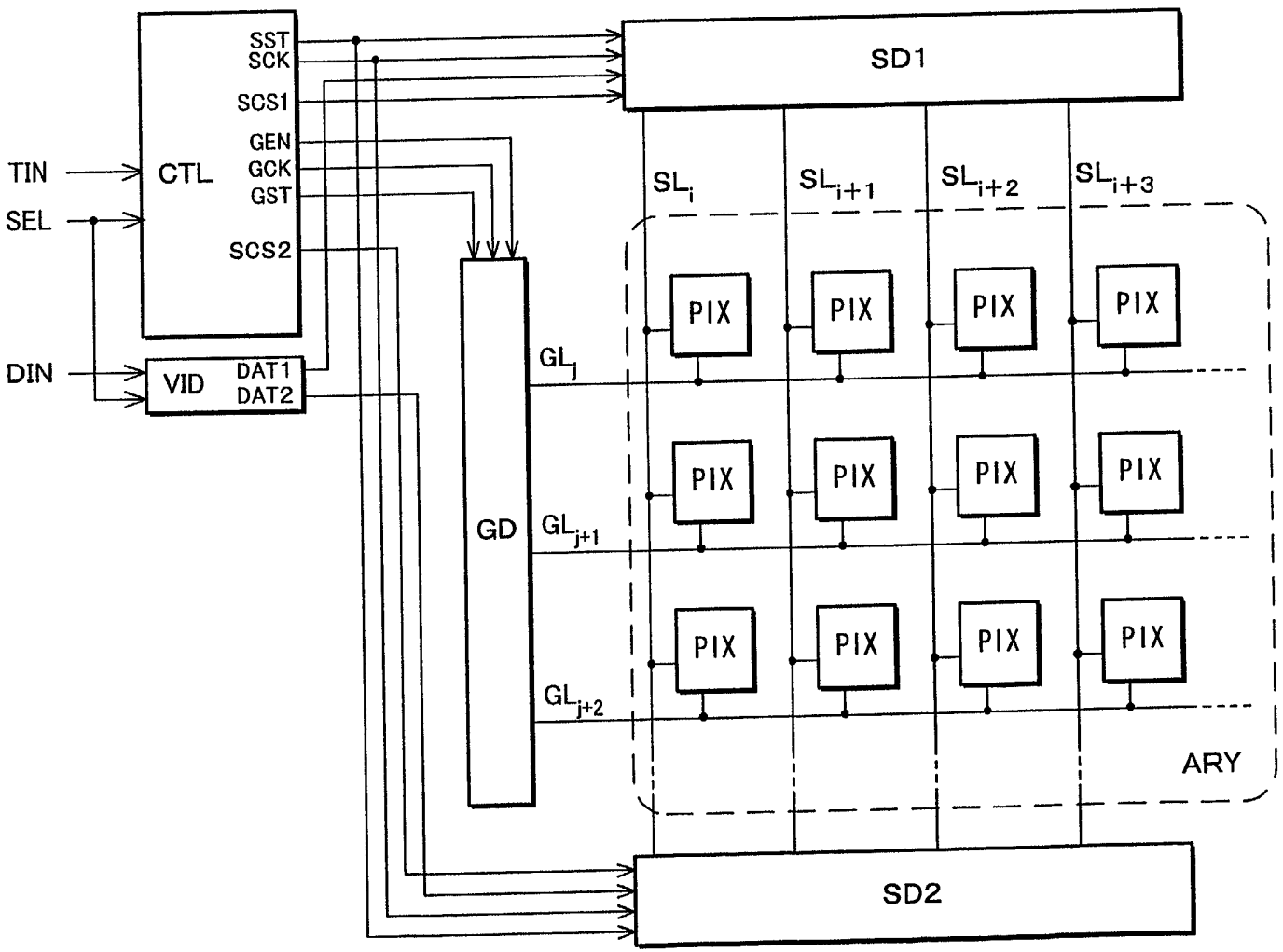
SST
SCK
SCS1
GEN
GCK
GST
SCS2
CTL
TIN
SEL
DIN
VID
DAT1
DAT2
SD1
SD2
GD
SL_i
SL_i+1
SL_i+2
SL_i+3
GL_j
GL_j+1
GL_j+2
PIX
ARY

FIG. 27

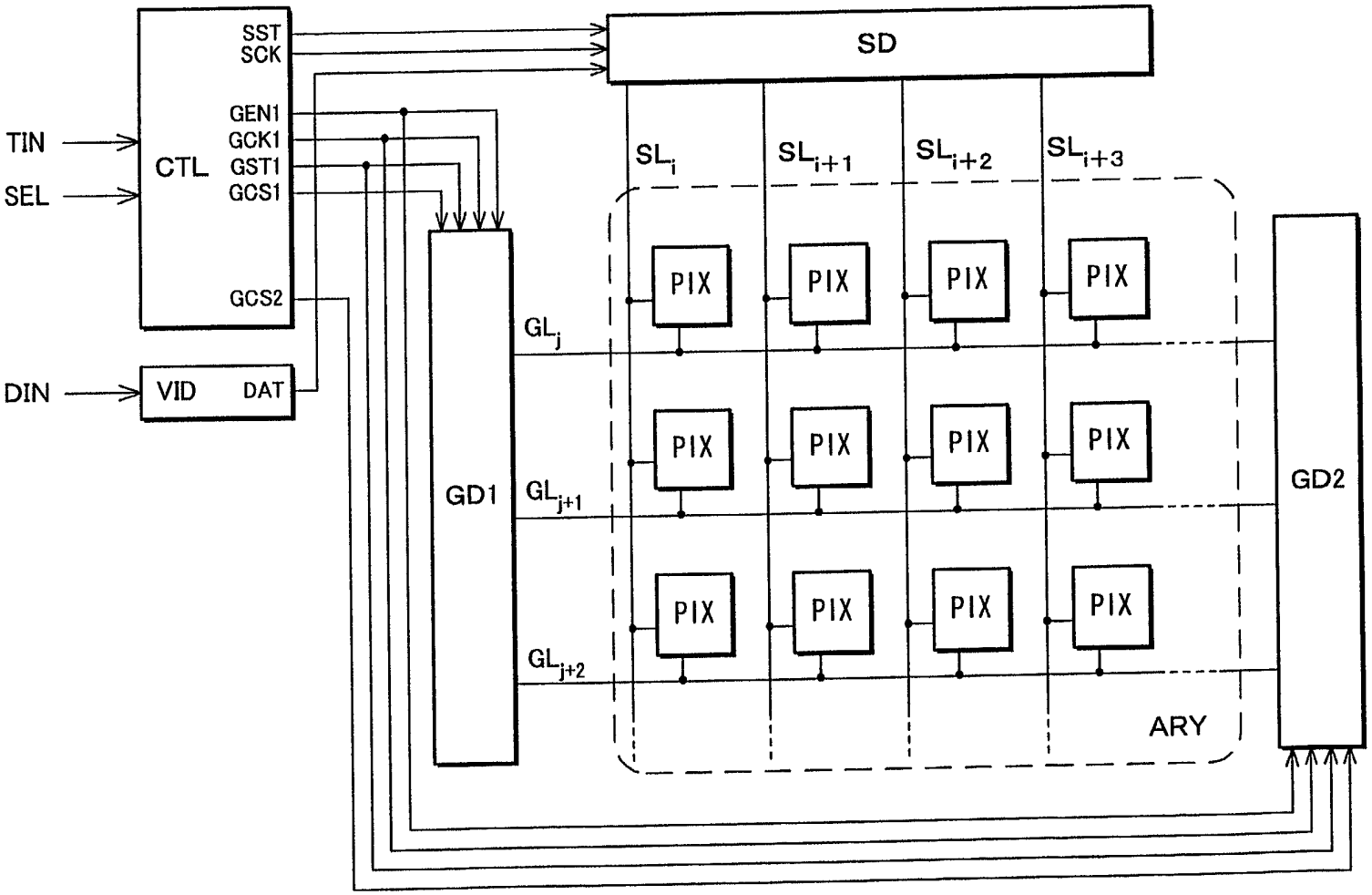
SST
SCK
SD
GEN1
GCK1
GST1
GCS1
TIN
SEL
CTL
GCS2
DIN
VID
DAT
SL_i
SL_i+1
SL_i+2
SL_i+3
GD1
GL_j
GL_j+1
GL_j+2
PIX
GD2
ARY

FIG. 28 (a)

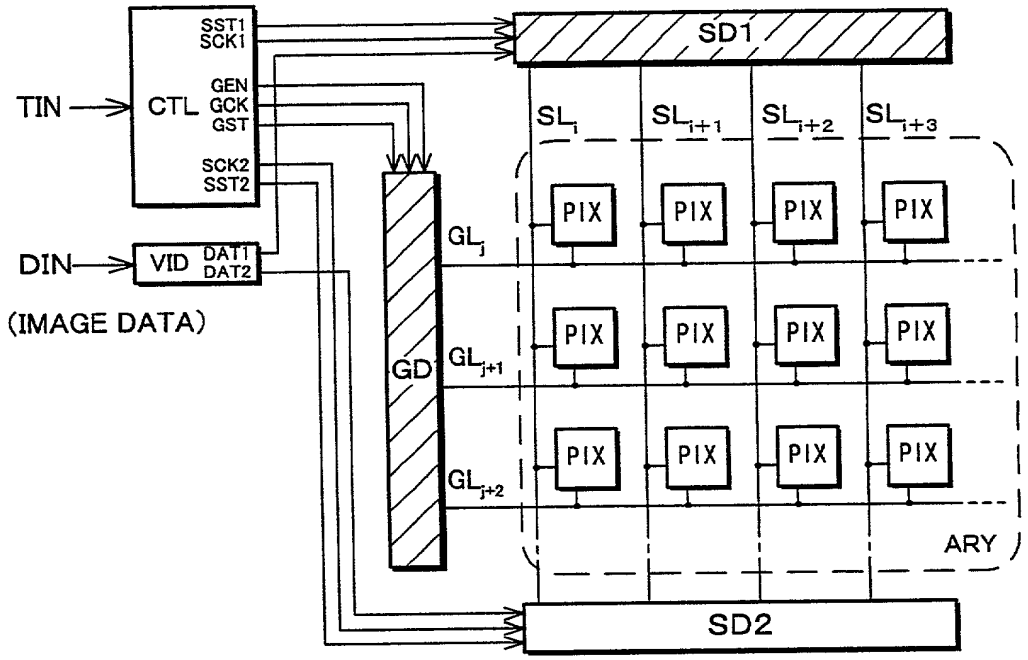

FIG. 28 (b)

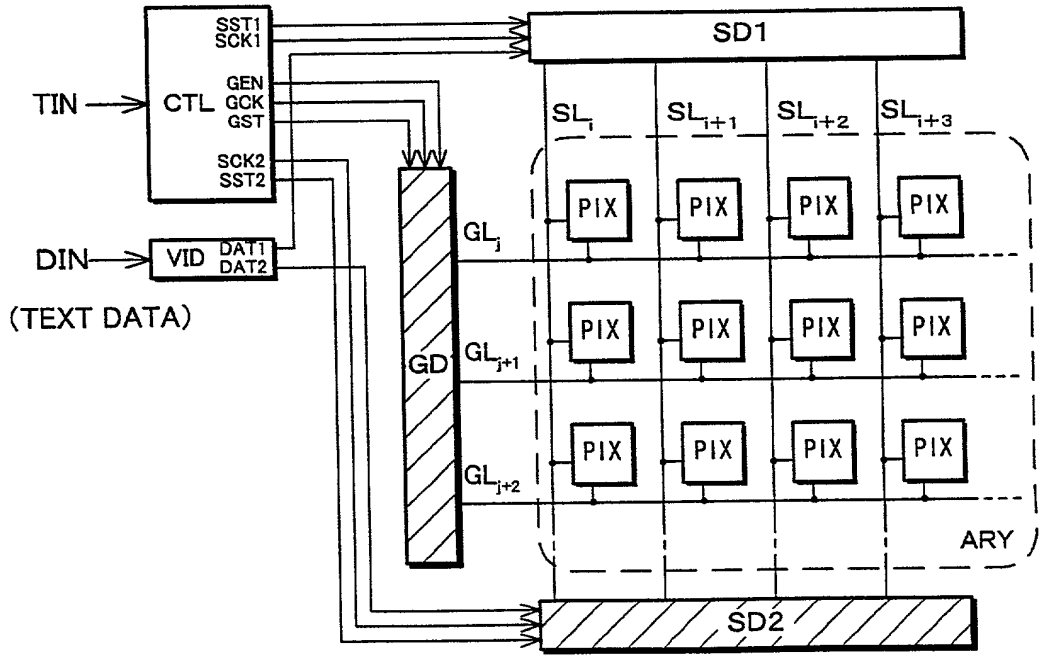

FIG. 29 (a)

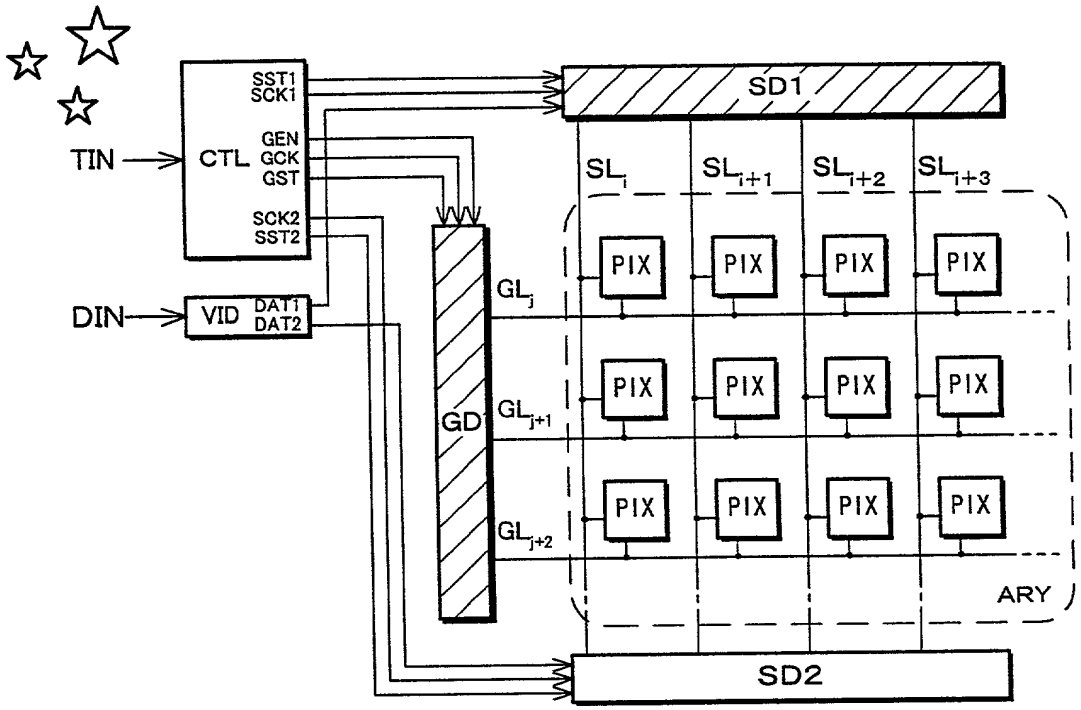

FIG. 29 (b)

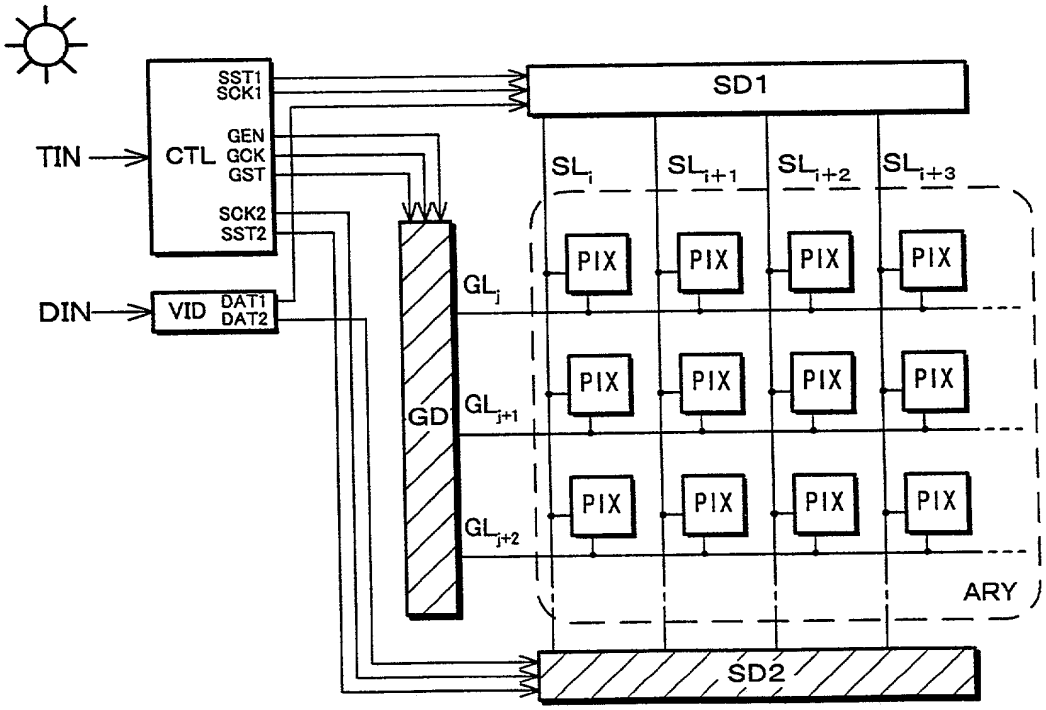

FIG. 30 (a)

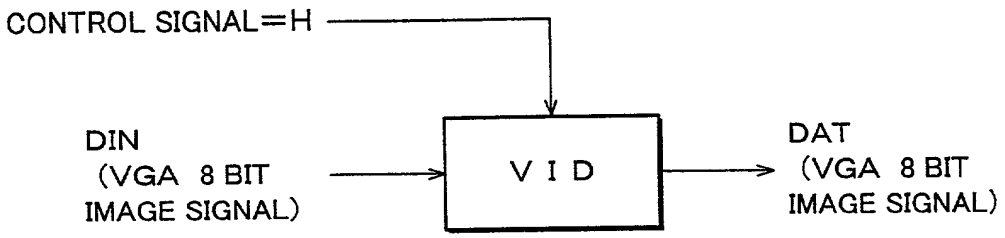

FIG. 30 (b)

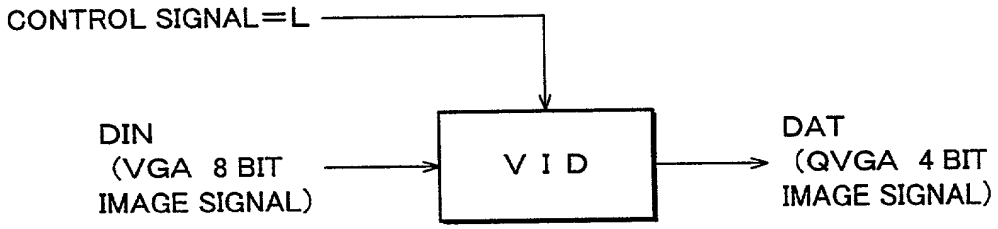

FIG. 31 (a)

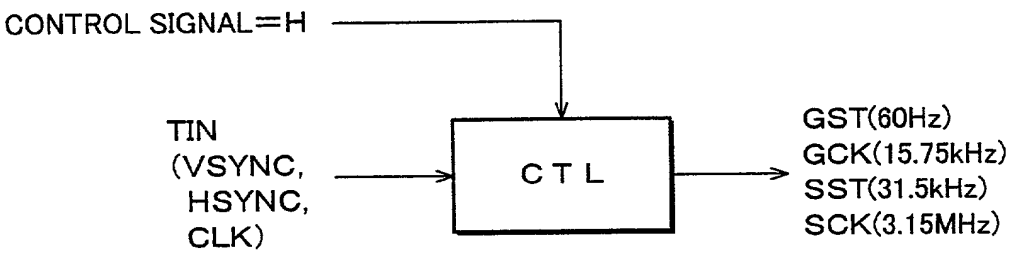

FIG. 31 (b)

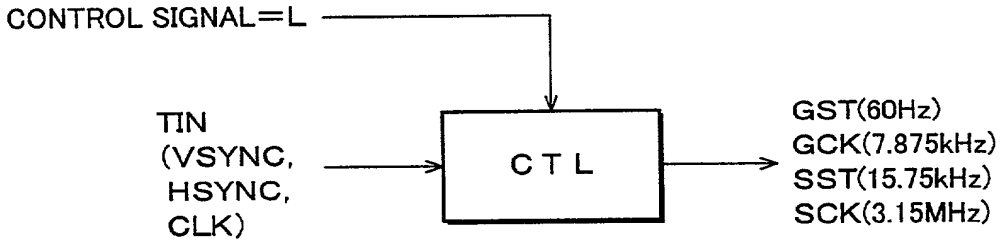

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FIG. 32

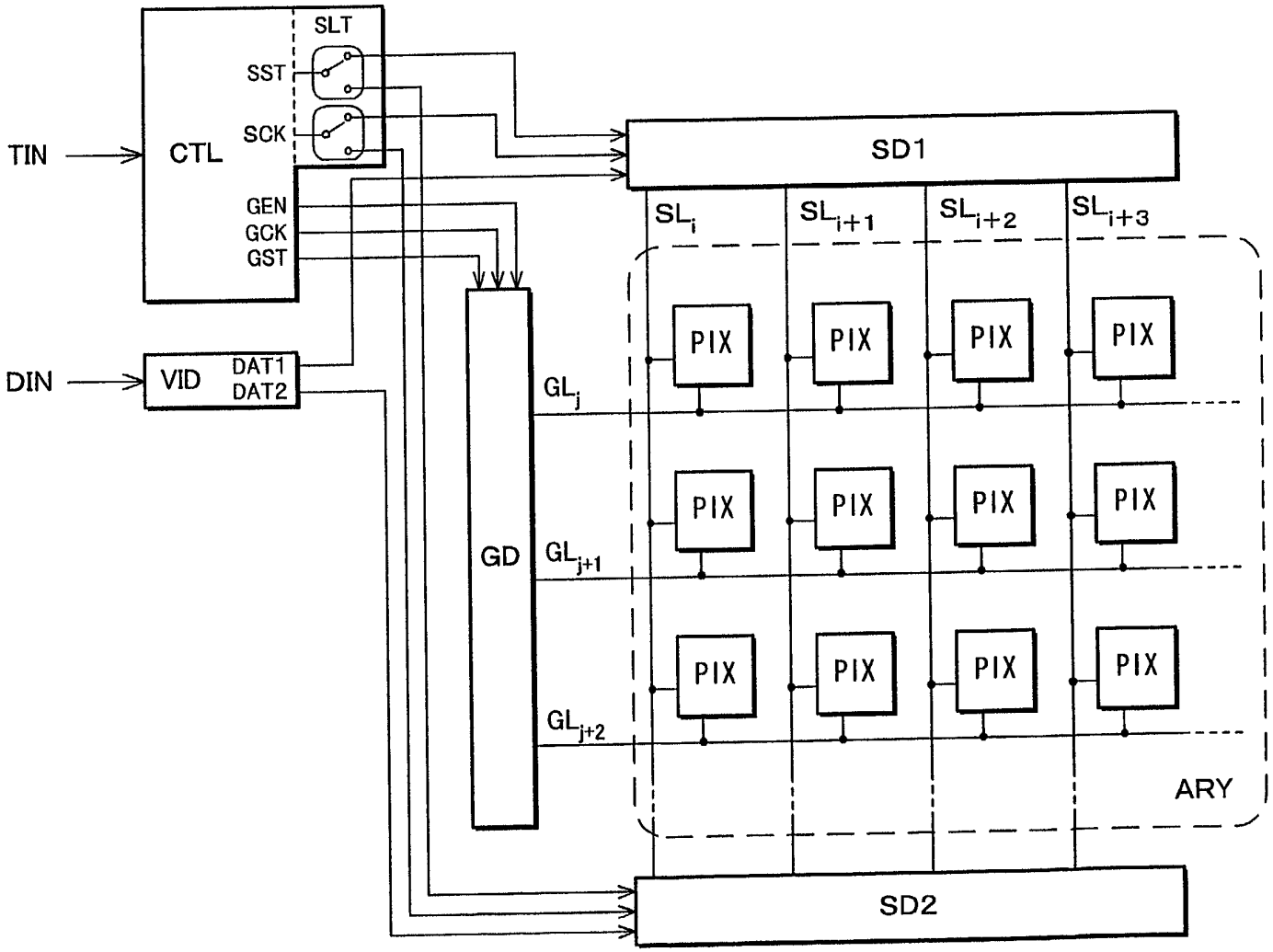
SLT
SST
SCK
TIN
CTL
GEN
GCK
GST
DIN
VID
DAT1
DAT2
SD1
SL_i
SL_i+1
SL_i+2
SL_i+3
GD
GL_j
GL_j+1
GL_j+2
PIX
ARY
SD2

FIG. 33

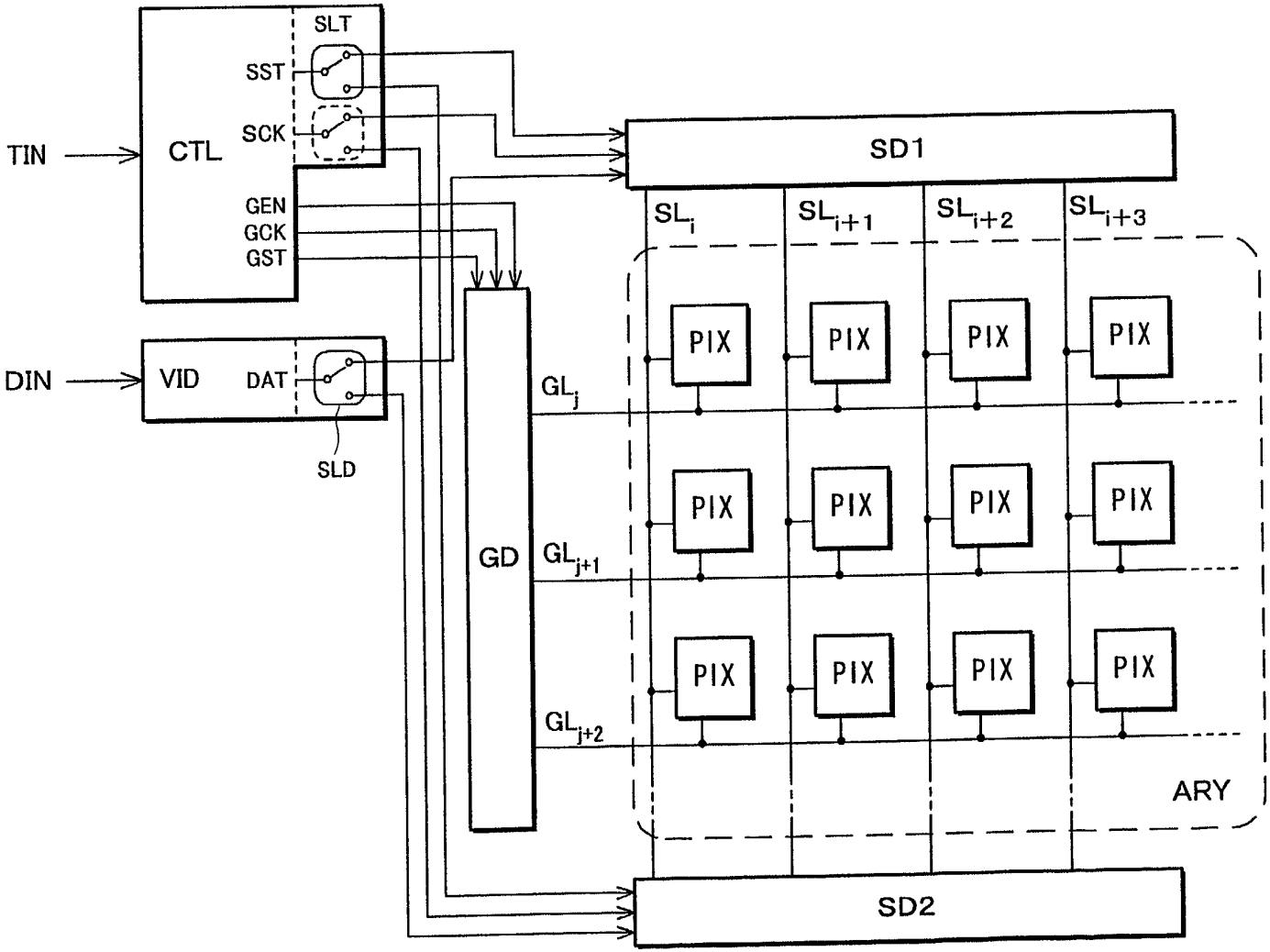
SLT
SST
SCK
TIN
CTL
GEN
GCK
GST
DIN
VID
DAT
SLD
GD
SD1
SD2
SL_i
SL_{i+1}
SL_{i+2}
SL_{i+3}
GL_j
GL_{j+1}
GL_{j+2}
PIX
ARY

FIG. 34

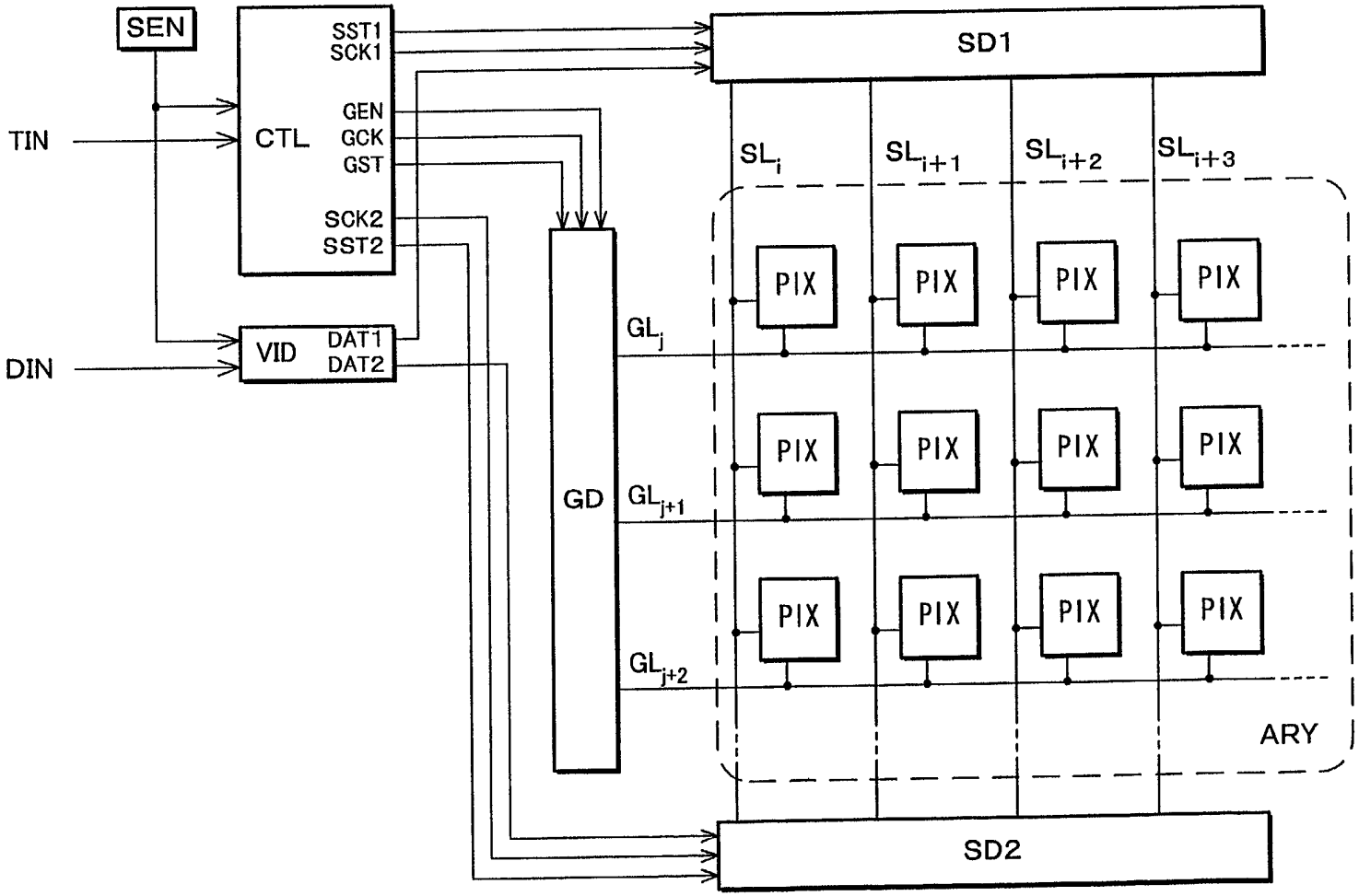
SEN
TIN
DIN
CTL
VID
SST1
SCK1
GEN
GCK
GST
SCK2
SST2
DAT1
DAT2
GD
SD1
SD2
SL_i
SL_i+1
SL_i+2
SL_i+3
GL_j
GL_j+1
GL_j+2
PIX
ARY

FIG. 35

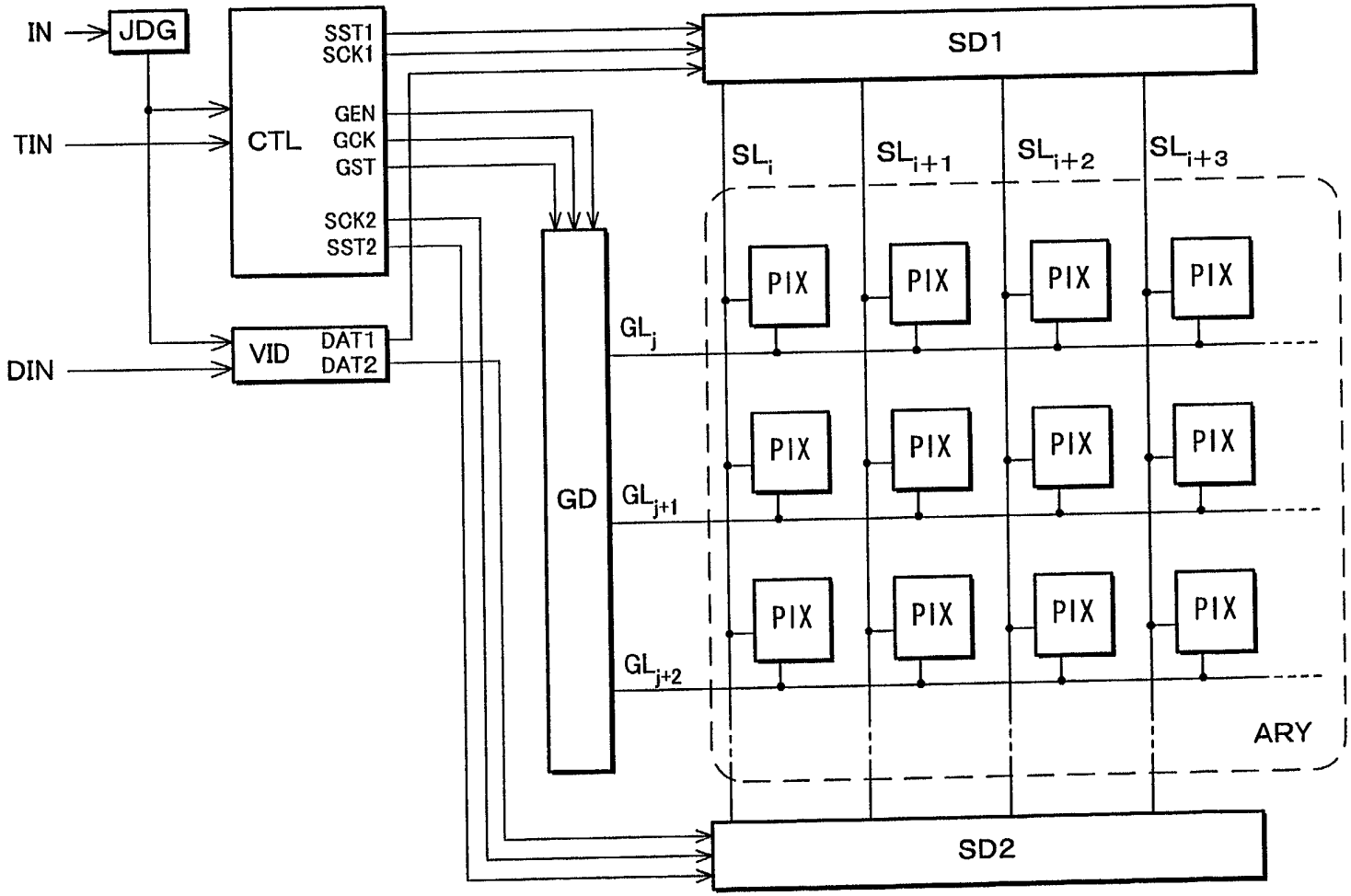
IN
JDG
TIN
DIN
CTL
VID
SST1
SCK1
GEN
GCK
GST
SCK2
SST2
DAT1
DAT2
GD
SD1
SD2
SL_i
SL_{i+1}
SL_{i+2}
SL_{i+3}
GL_j
GL_{j+1}
GL_{j+2}
PIX
ARY

FIG. 36

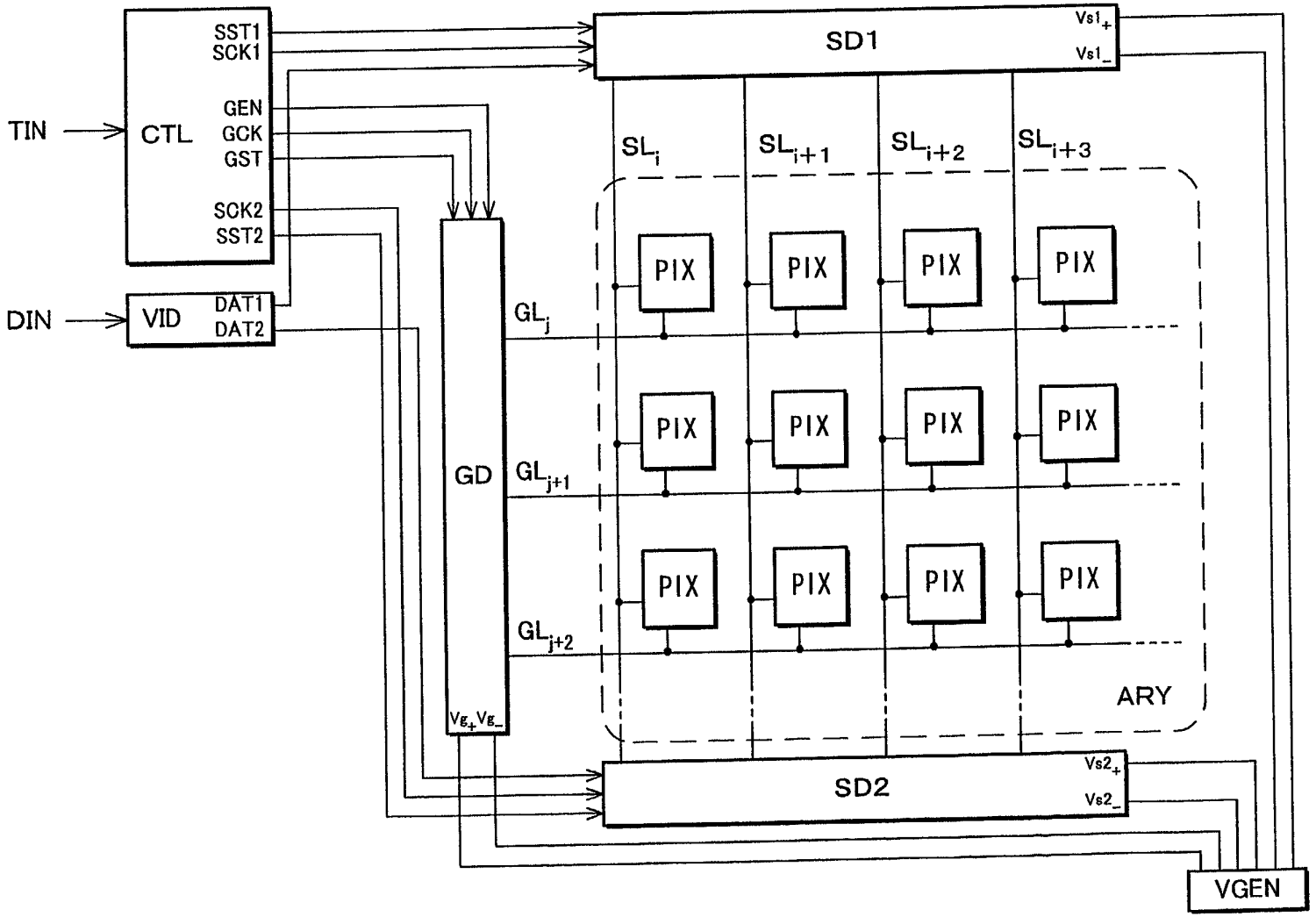
TIN
DIN
CTL
VID
SST1
SCK1
GEN
GCK
GST
SCK2
SST2
DAT1
DAT2
GD
SD1
SD2
Vs1+
Vs1-
Vs2+
Vs2-
Vg+Vg-
SLi
SLi+1
SLi+2
SLi+3
GLj
GLj+1
GLj+2
PIX
ARY
VGEN

FIG. 37

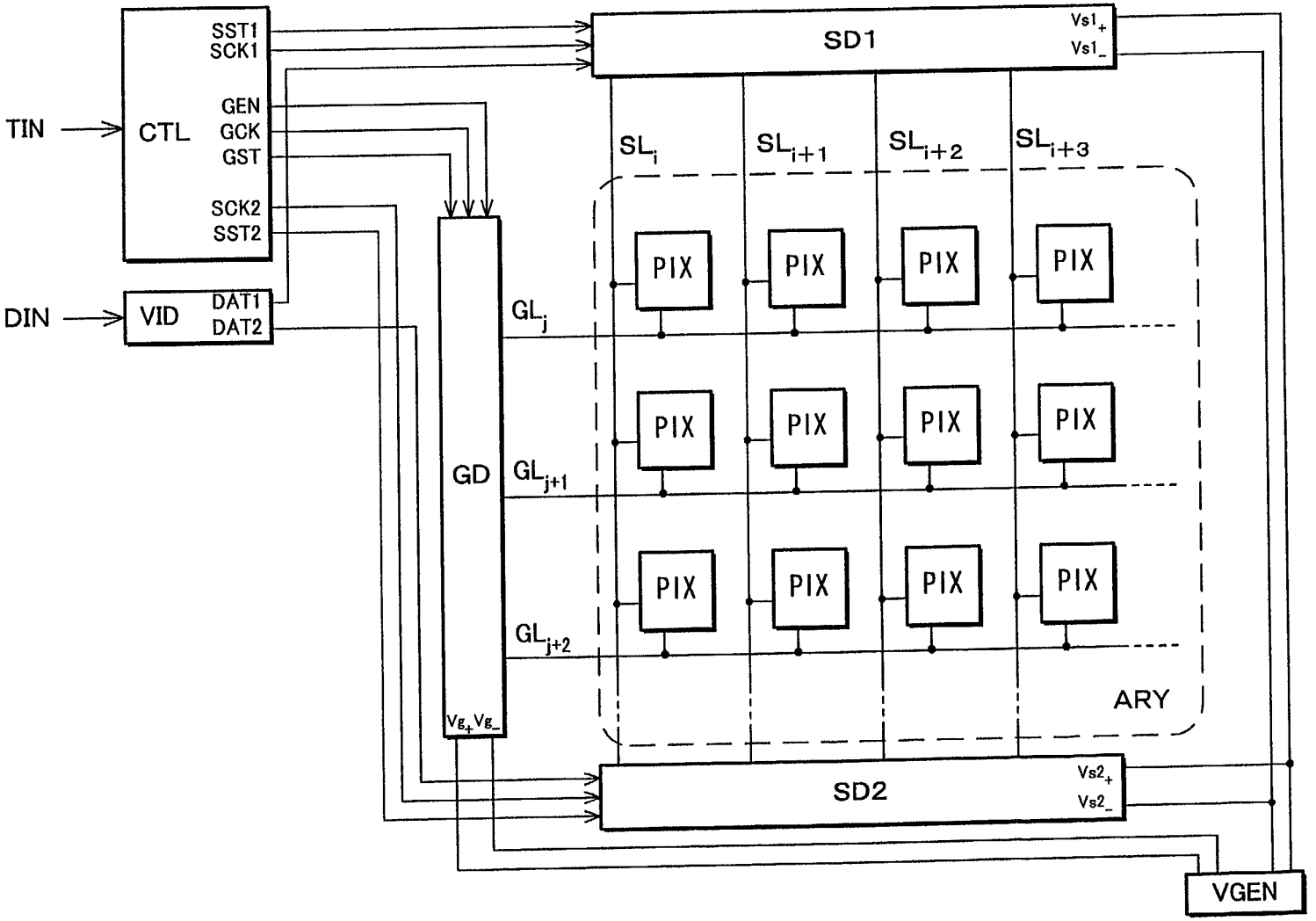
TIN
CTL
SST1
SCK1
GEN
GCK
GST
SCK2
SST2
DIN
VID
DAT1
DAT2
SD1
Vs1+
Vs1-
SL_i
SL_i+1
SL_i+2
SL_i+3
PIX
GL_j
GL_j+1
GL_j+2
GD
Vg+ Vg-
ARY
SD2
Vs2+
Vs2-
VGEN

FIG. 38

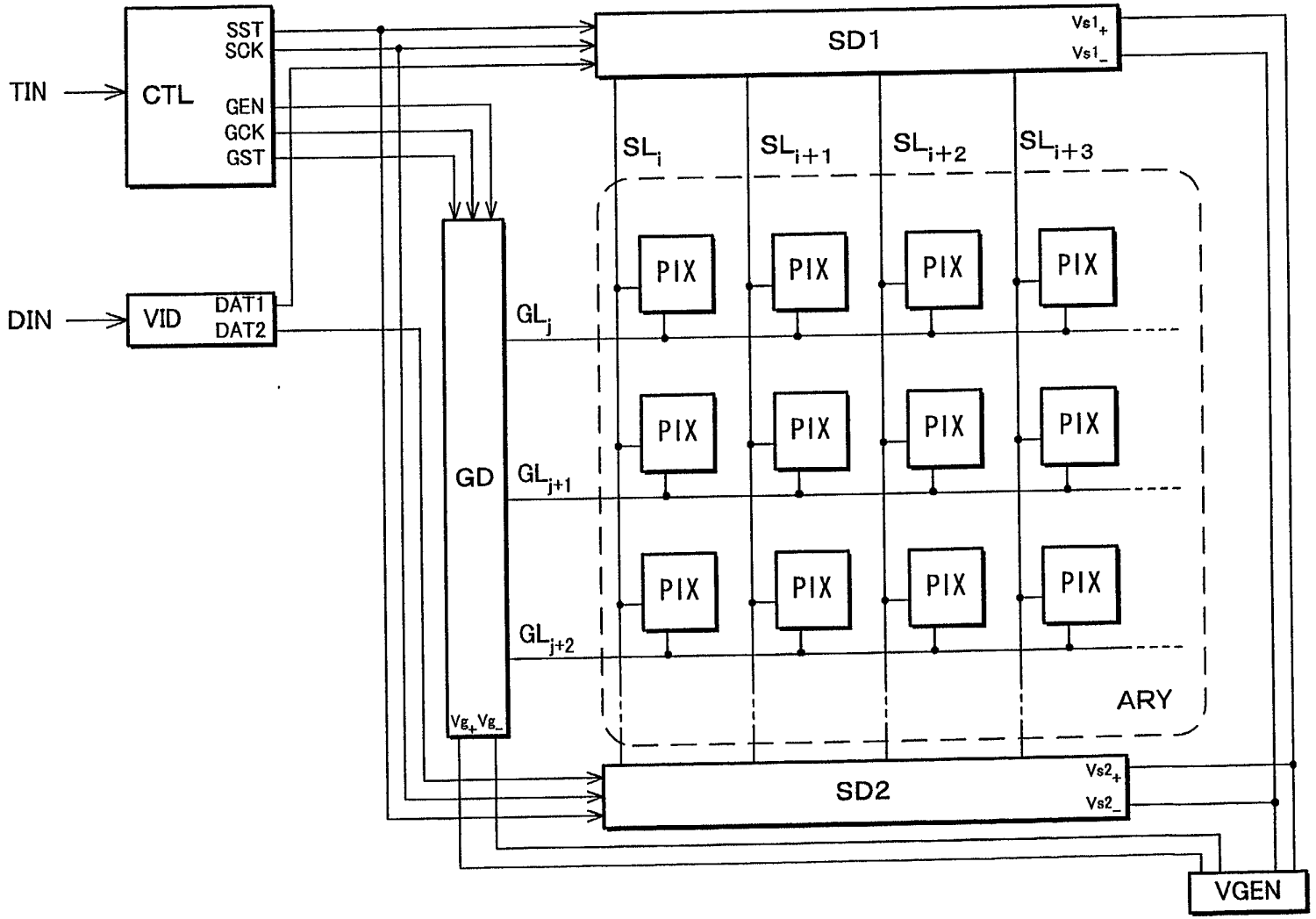
TIN
CTL
SST
SCK
GEN
GCK
GST
DIN
VID
DAT1
DAT2
SD1
Vs1+
Vs1-
SLi
SLi+1
SLi+2
SLi+3
PIX
GD
GLj
GLj+1
GLj+2
Vg+ Vg-
ARY
SD2
Vs2+
Vs2-
VGEN

FIG. 39

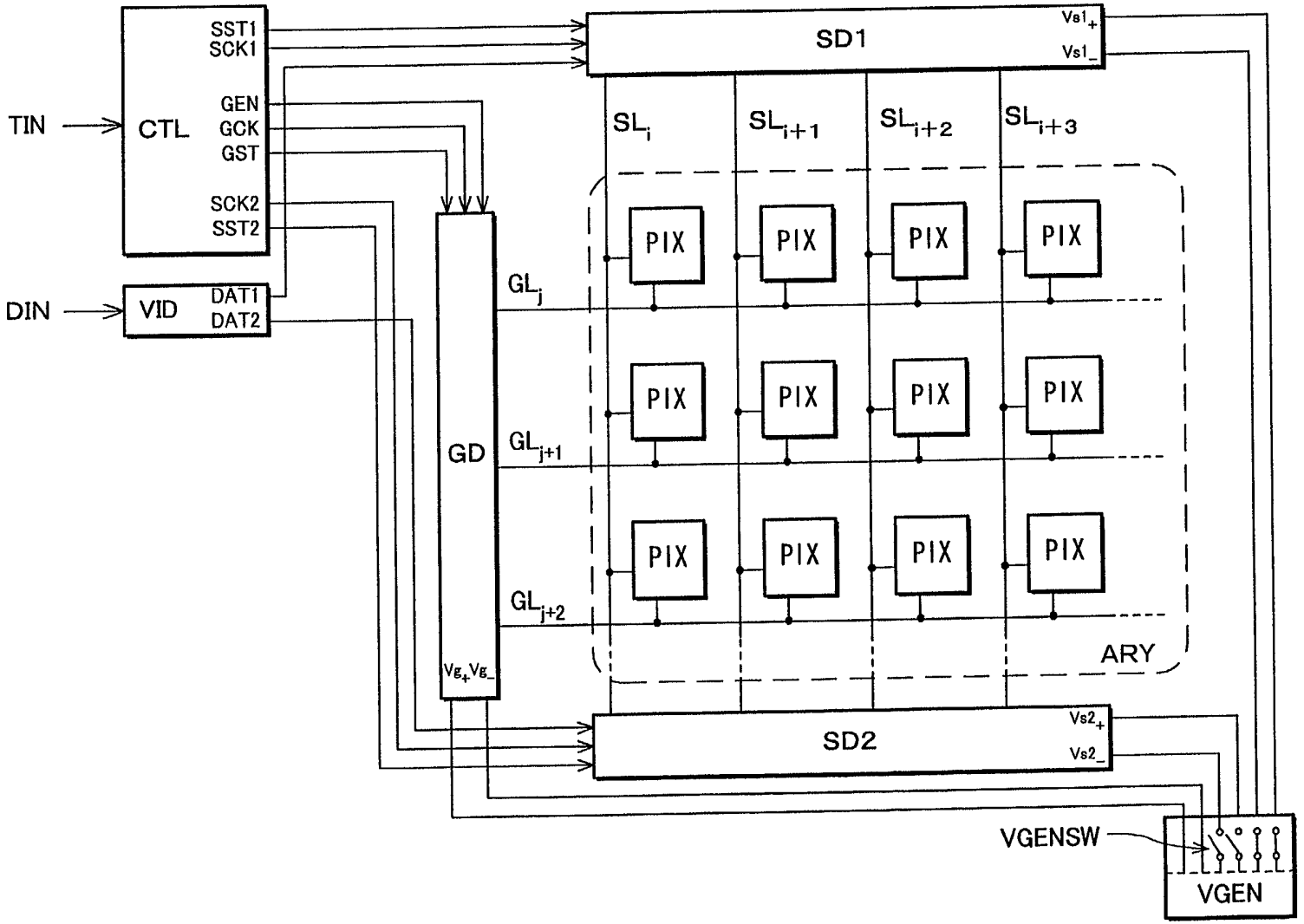
SST1
SCK1
GEN
GCK
GST
SCK2
SST2
TIN
CTL
DIN
VID
DAT1
DAT2
SD1
Vs1+
Vs1-
SLi
SLi+1
SLi+2
SLi+3
PIX
GLj
GLj+1
GLj+2
GD
Vg+Vg-
ARY
SD2
Vs2+
Vs2-
VGENSW
VGEN

FIG. 40

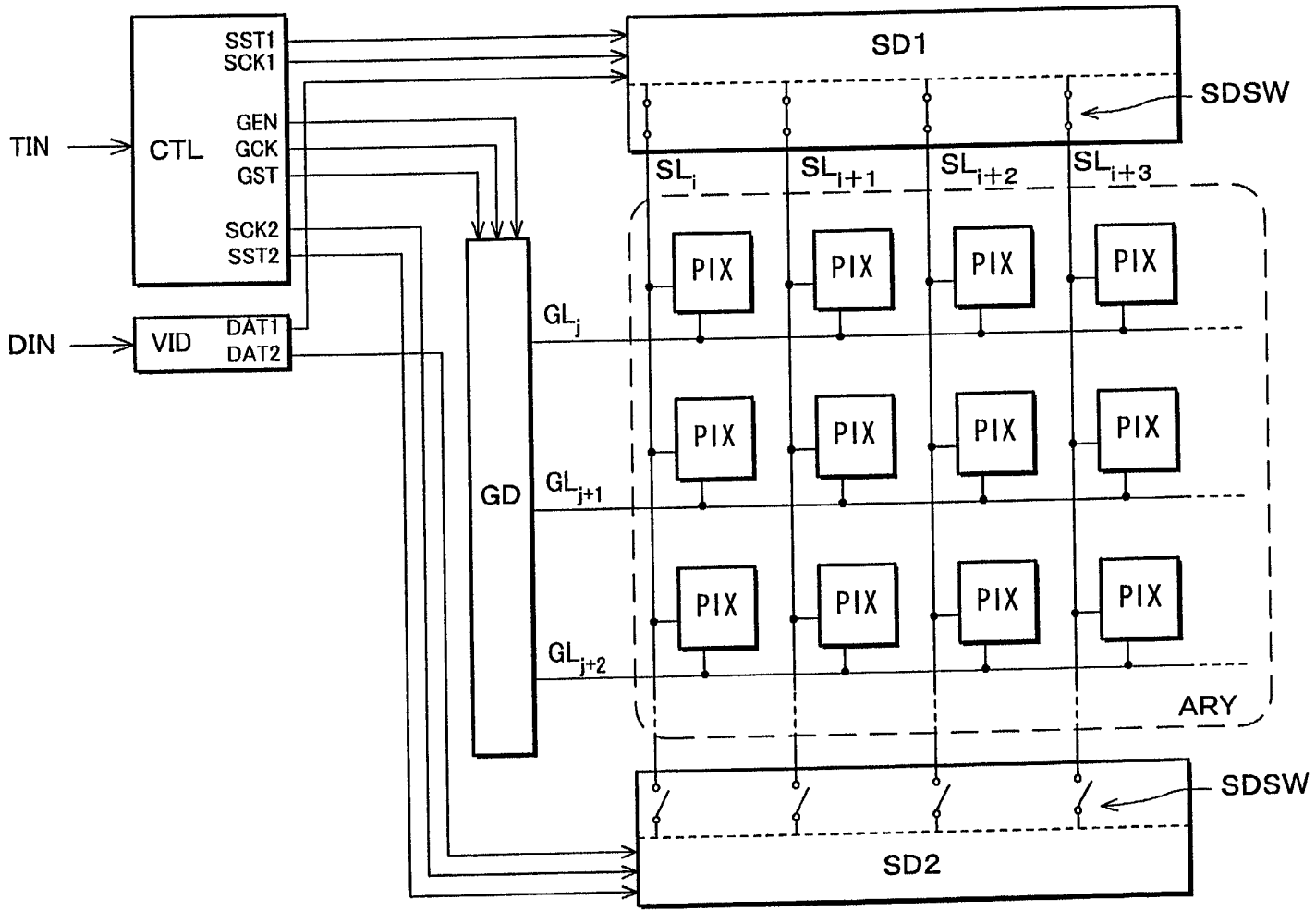
SST1
SCK1
GEN
GCK
GST
SCK2
SST2
TIN
CTL
DIN
VID
DAT1
DAT2
SD1
SDSW
SL_i
SL_i+1
SL_i+2
SL_i+3
PIX
GD
GL_j
GL_j+1
GL_j+2
ARY
SDSW
SD2

FIG. 41

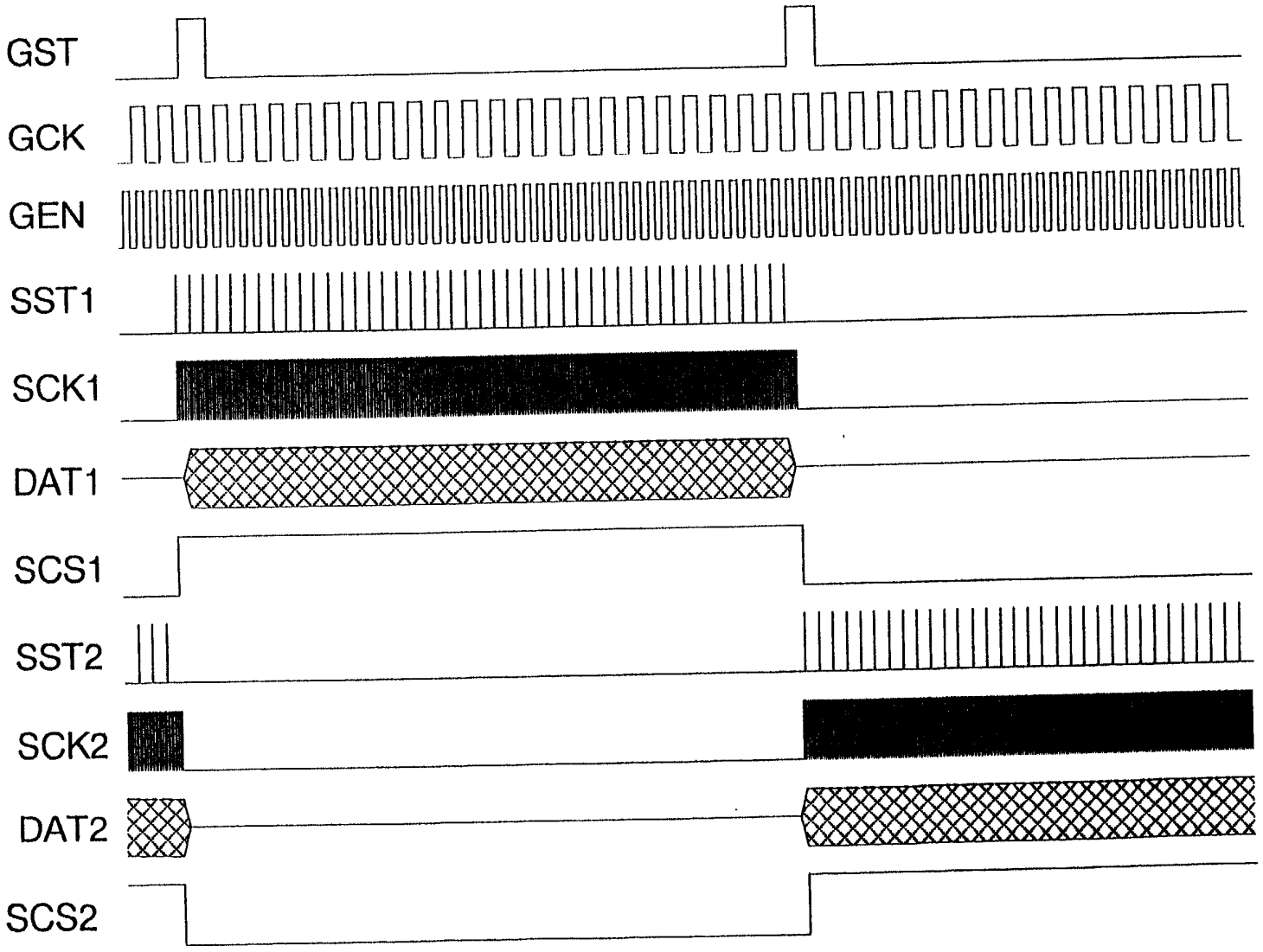

FIG. 42

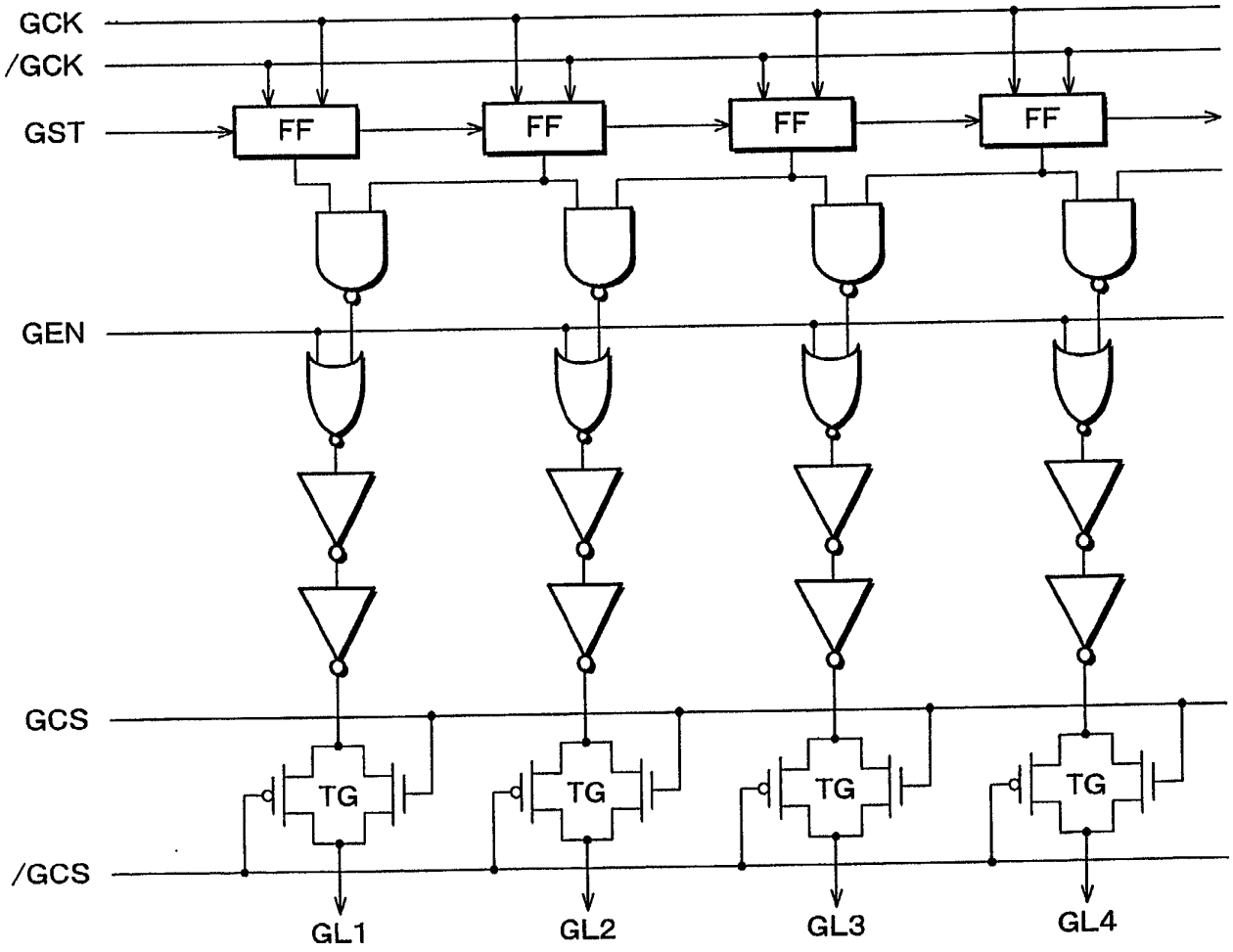

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FIG. 43 (a)

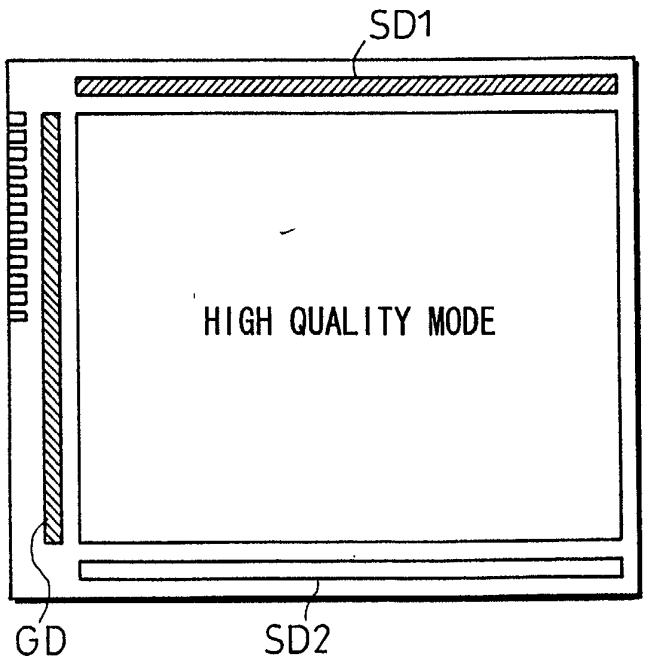

FIG. 43 (b)

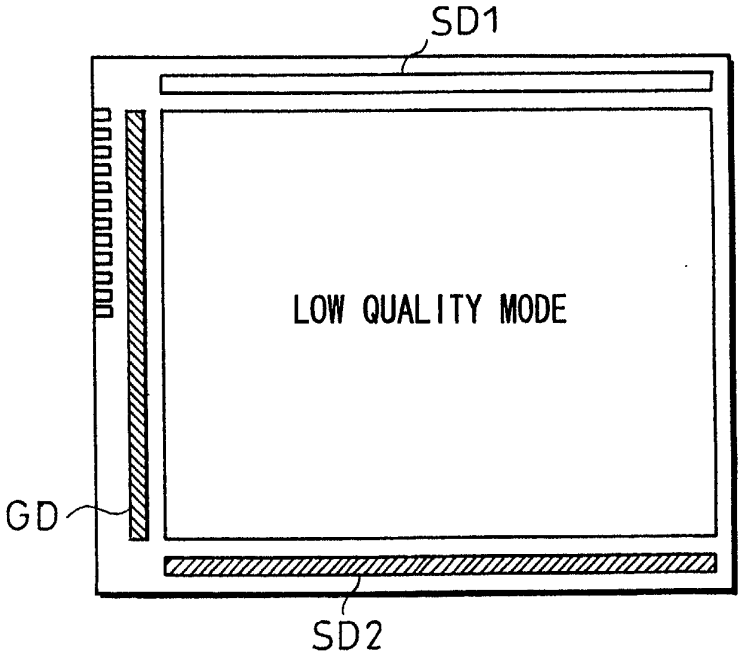

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FIG. 44 (a)

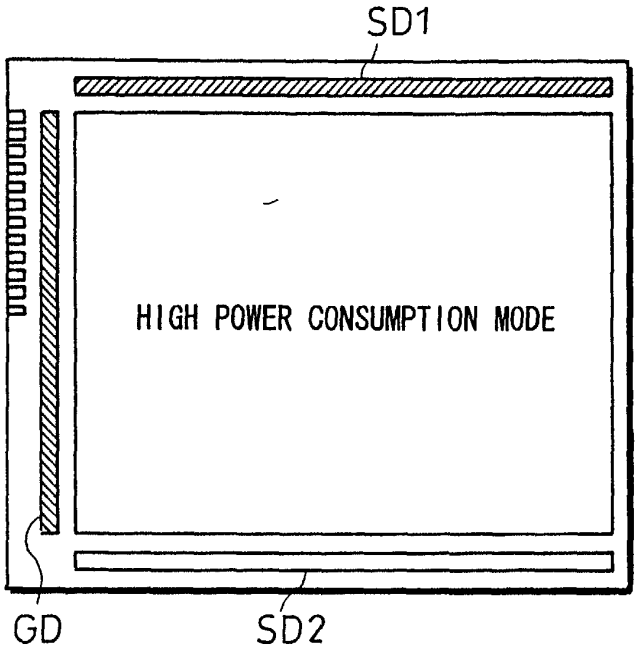

FIG. 44 (b)

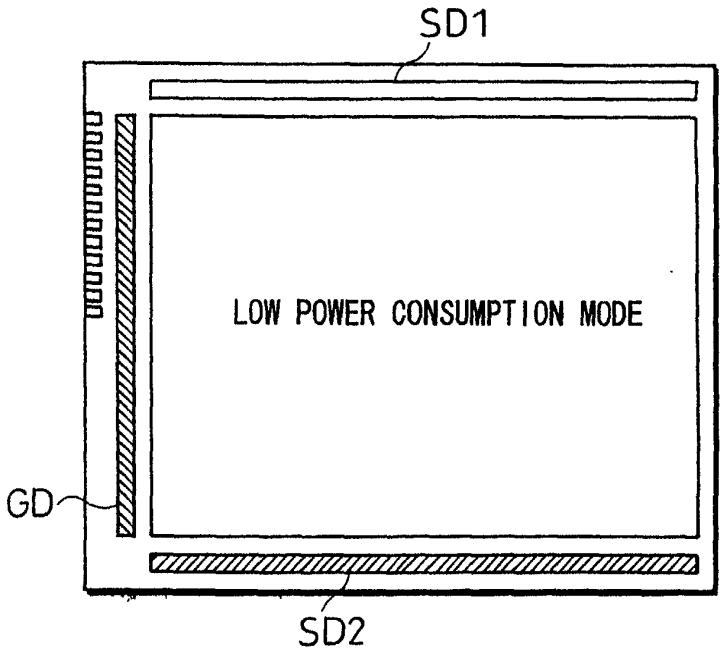

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FIG. 45(a)

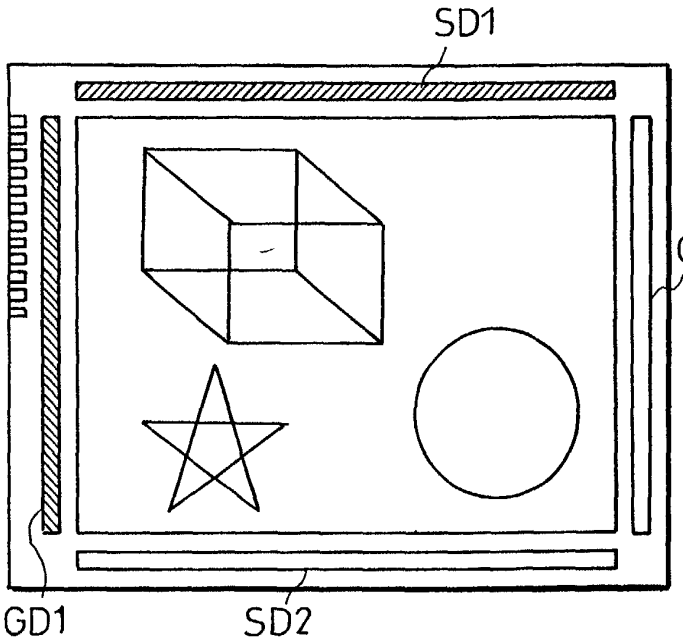


FIG. 45(b)

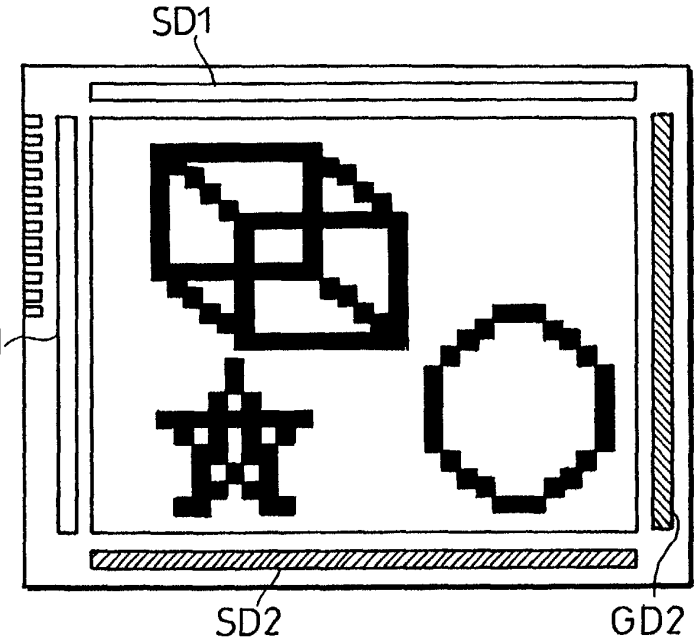


FIG. 46

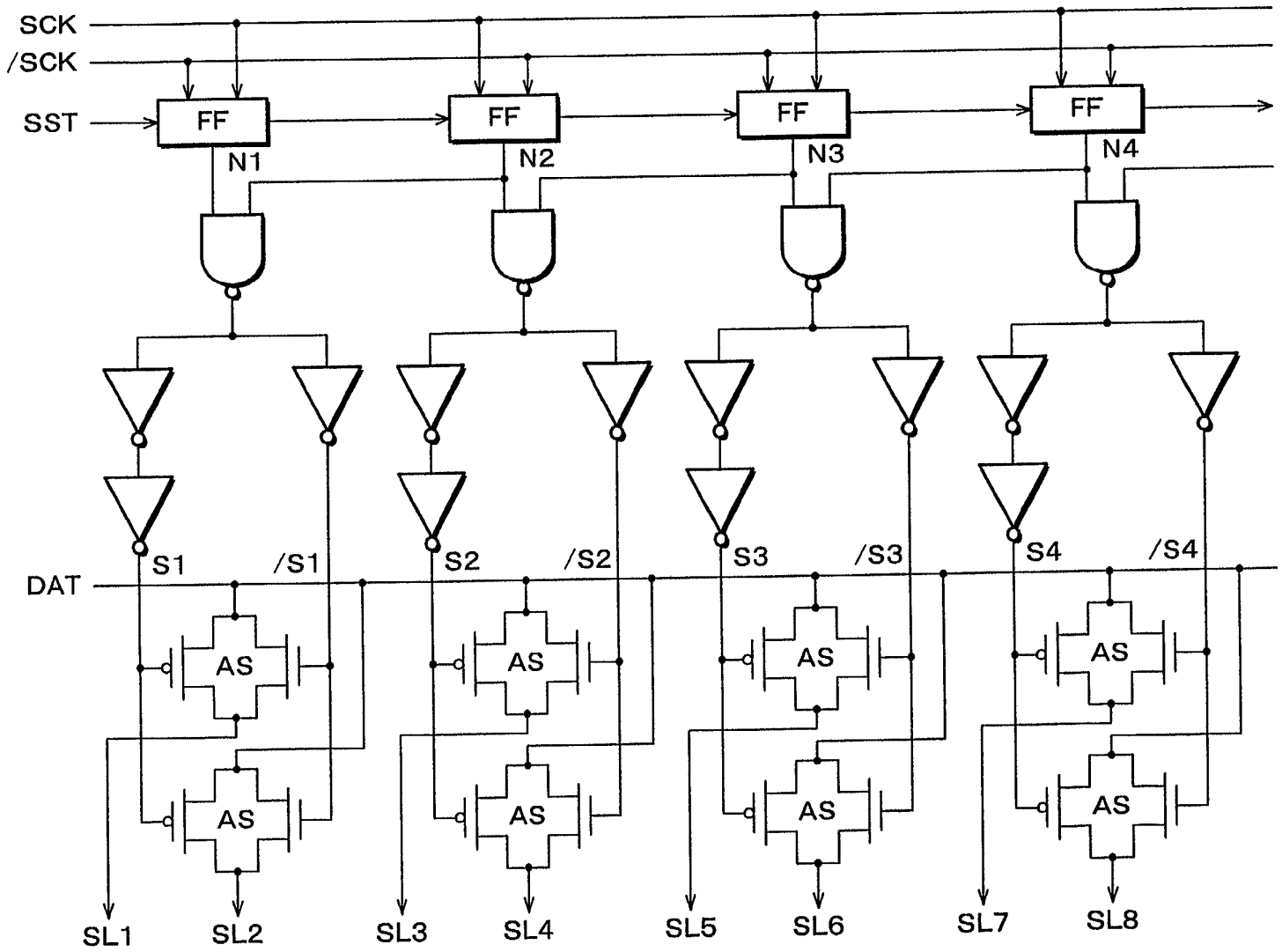
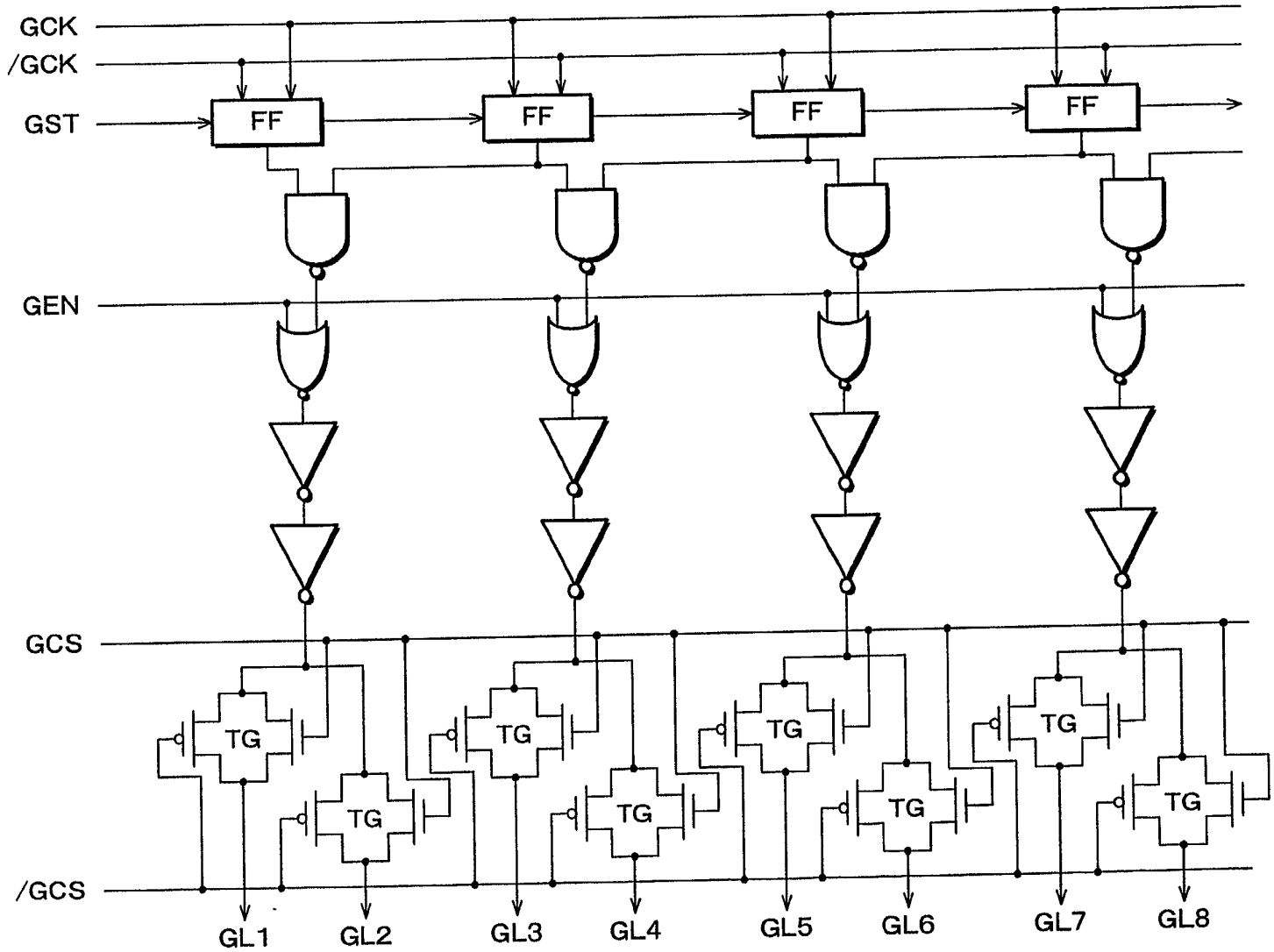

SCK
/SCK
SST
FF
FF
FF
FF
N1
N2
N3
N4
S1
/S1
S2
/S2
S3
/S3
S4
/S4
DAT
AS
SL1
SL2
SL3
SL4
SL5
SL6
SL7
SL8

FIG. 47


GCK
/GCK
GST
FF
FF
FF
FF
GEN
GCS
TG
TG
TG
TG
TG
TG
TG
TG
/GCS
GL1
GL2
GL3
GL4
GL5
GL6
GL7
GL8

F I G. 4 8

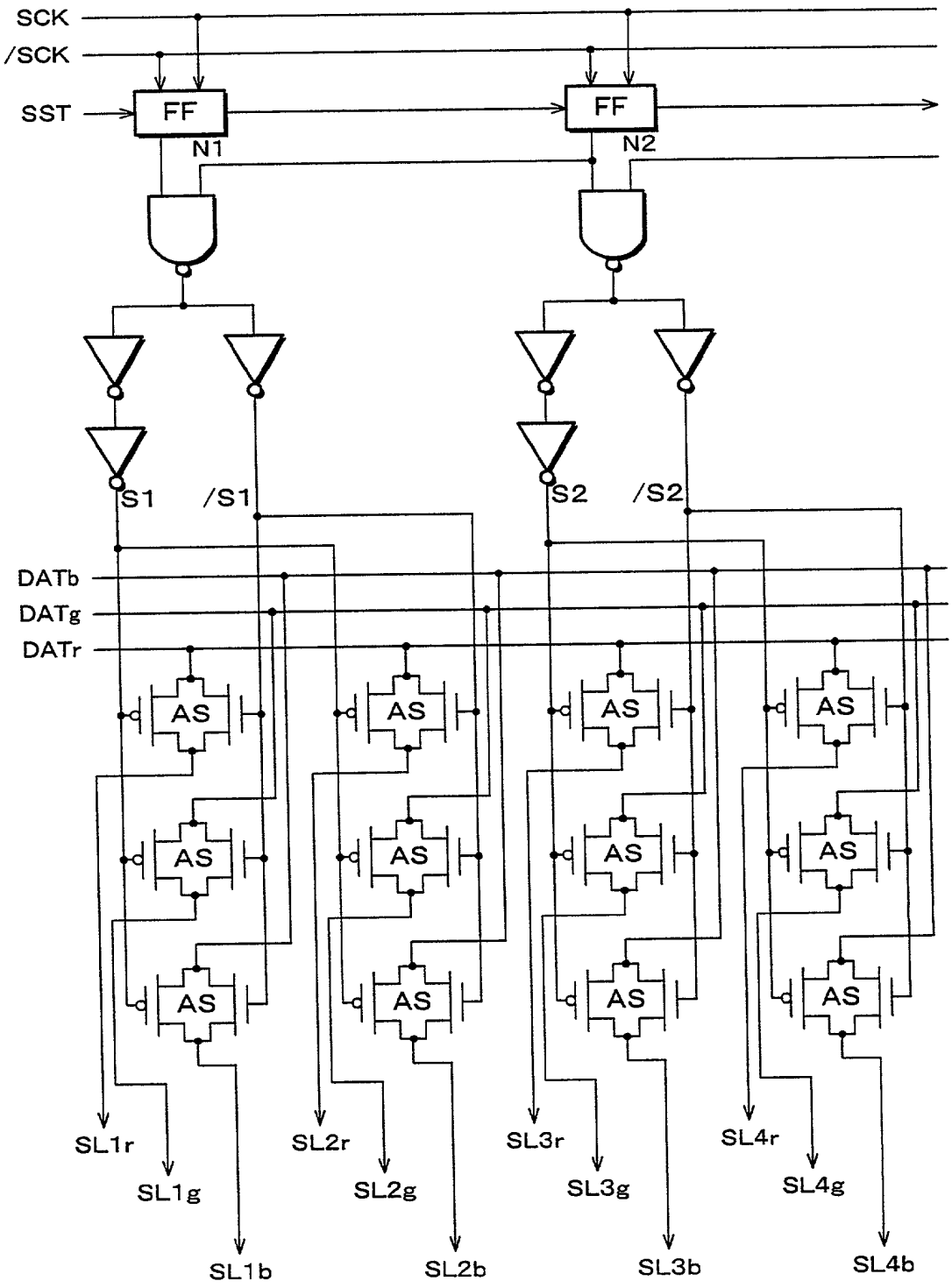

SCK
/SCK
SST
FF
N1
FF
N2
S1
/S1
S2
/S2
DATb
DATg
DATr
AS
SL1r
SL1g
SL1b
SL2r
SL2g
SL2b
SL3r
SL3g
SL3b
SL4r
SL4g
SL4b

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FIG. 49

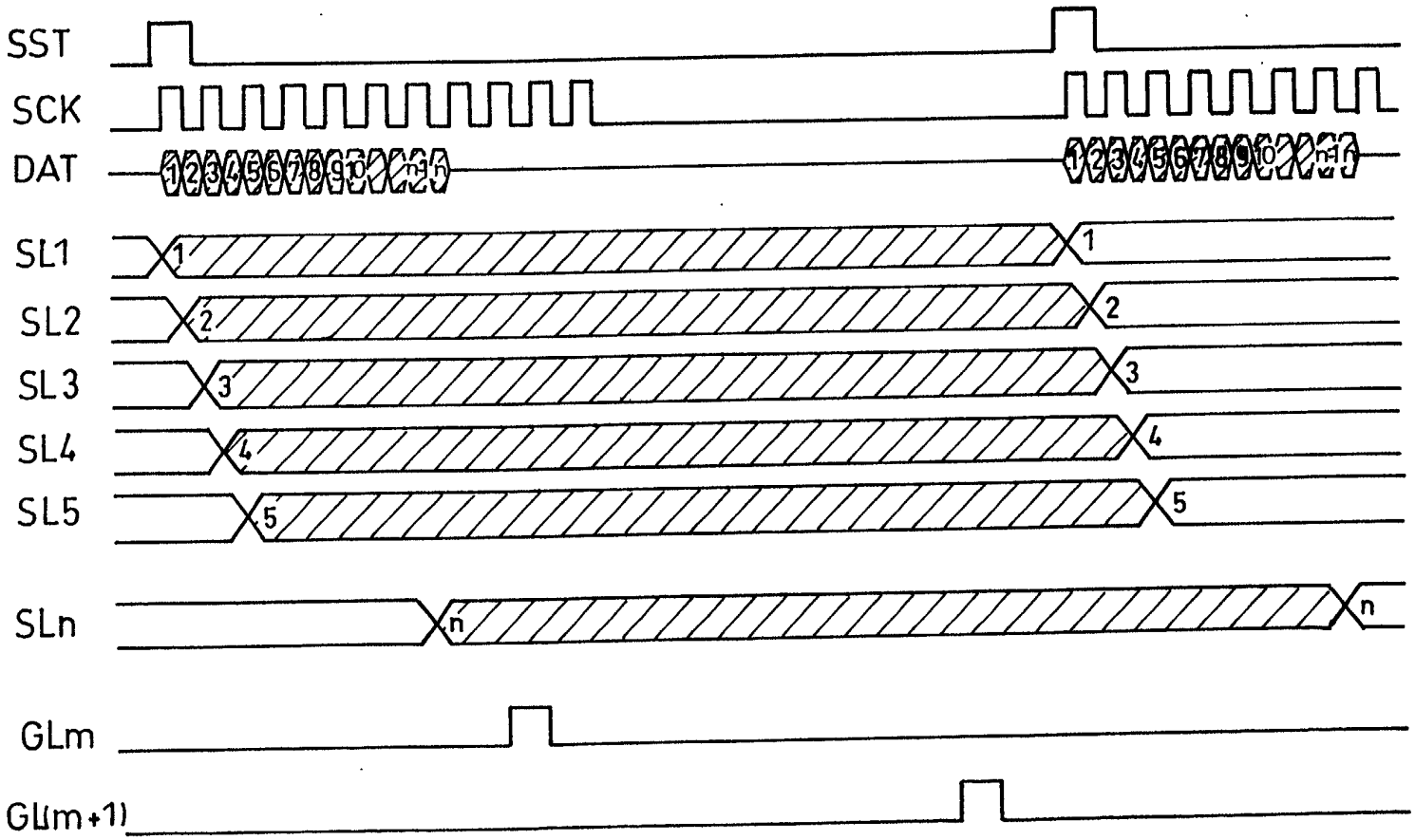

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FIG. 50

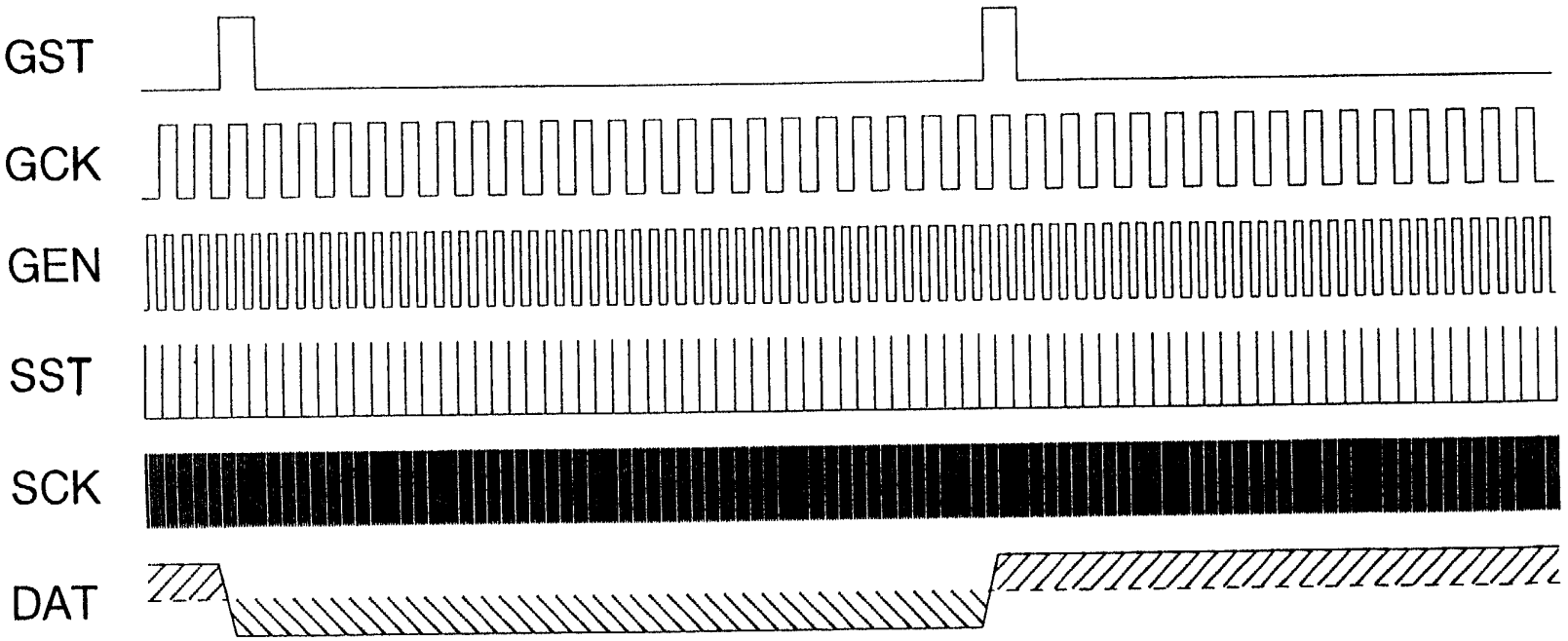

FIG. 51

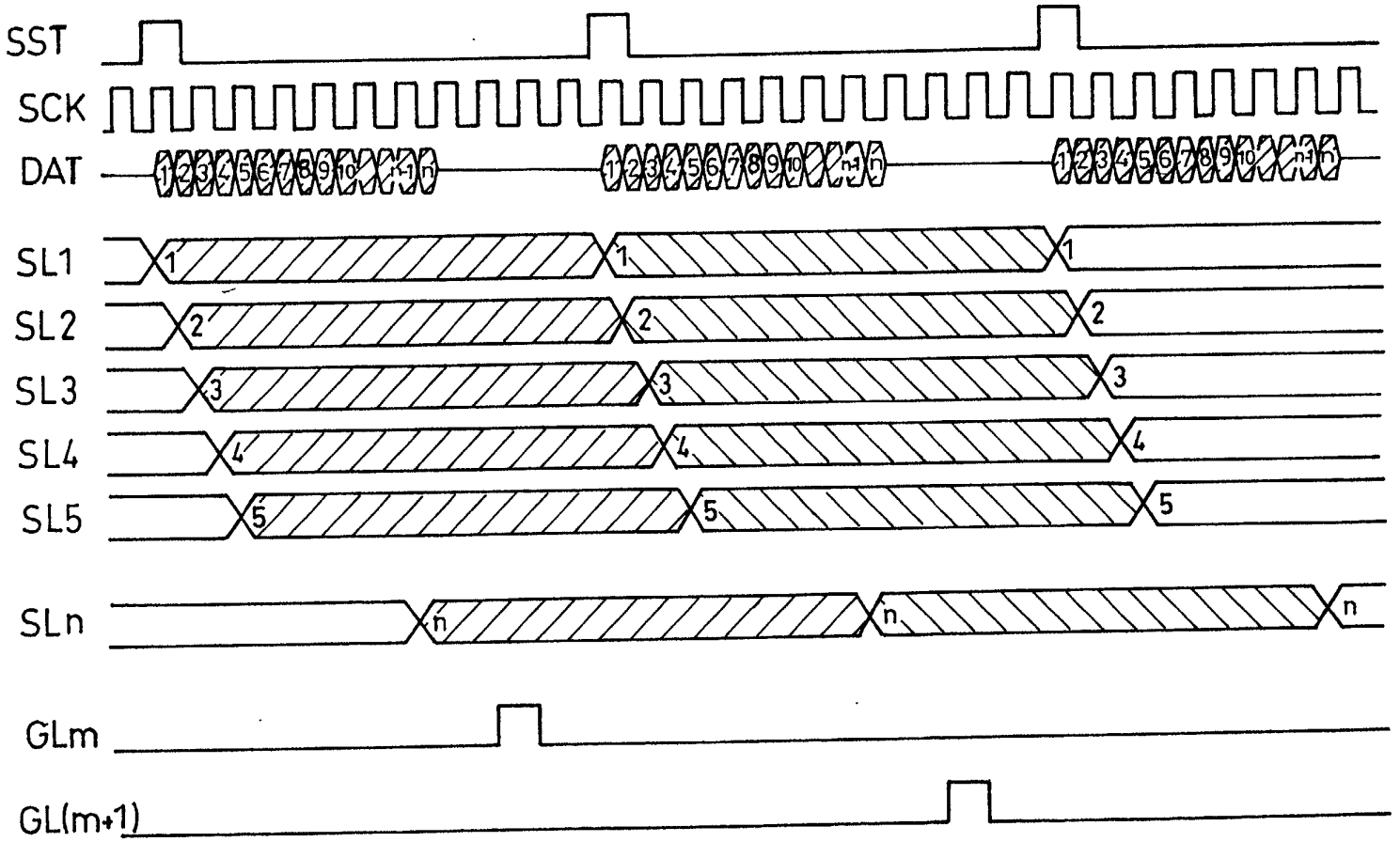

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FIG. 52

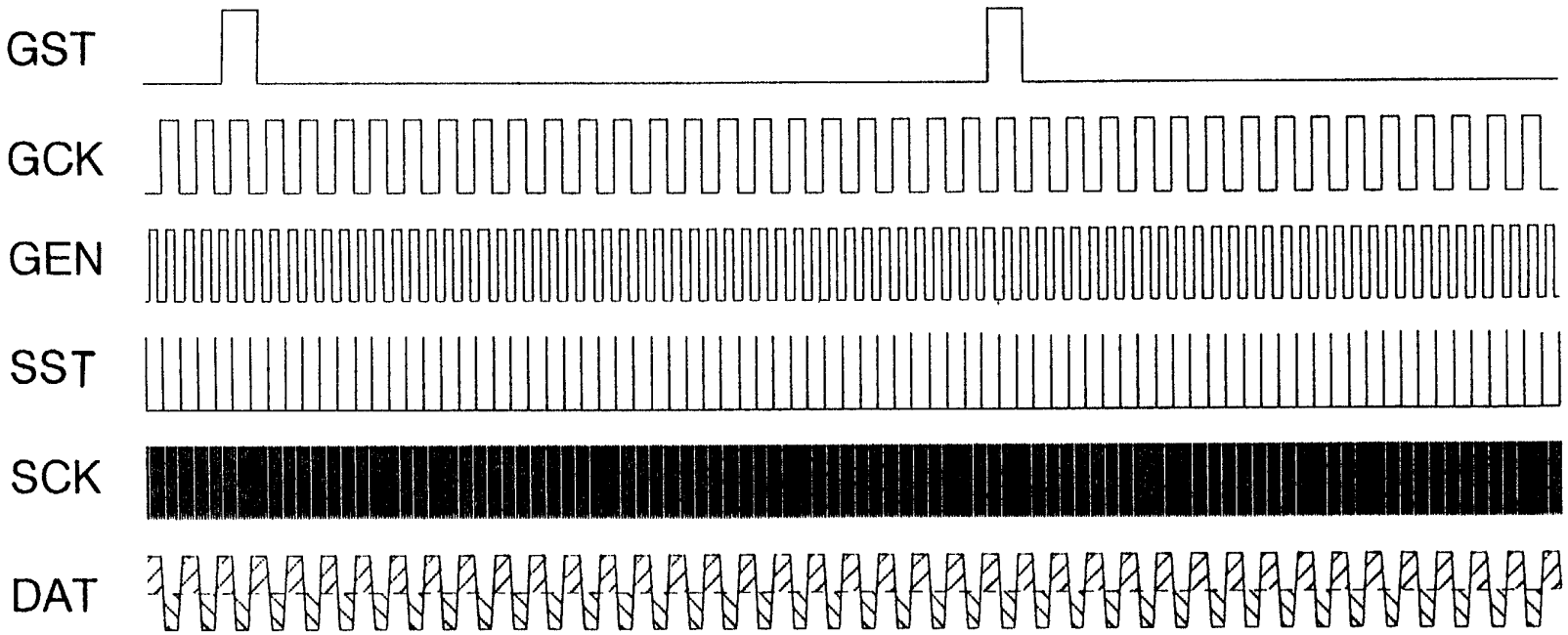

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FIG. 53 (a)

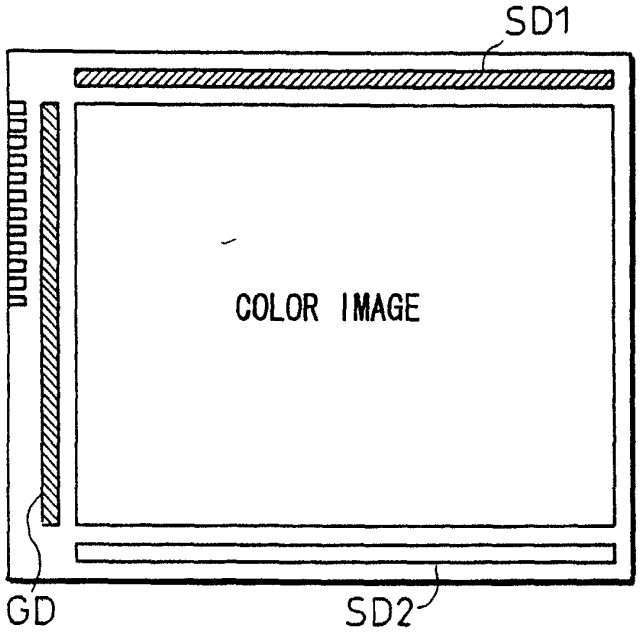

FIG. 53 (b)

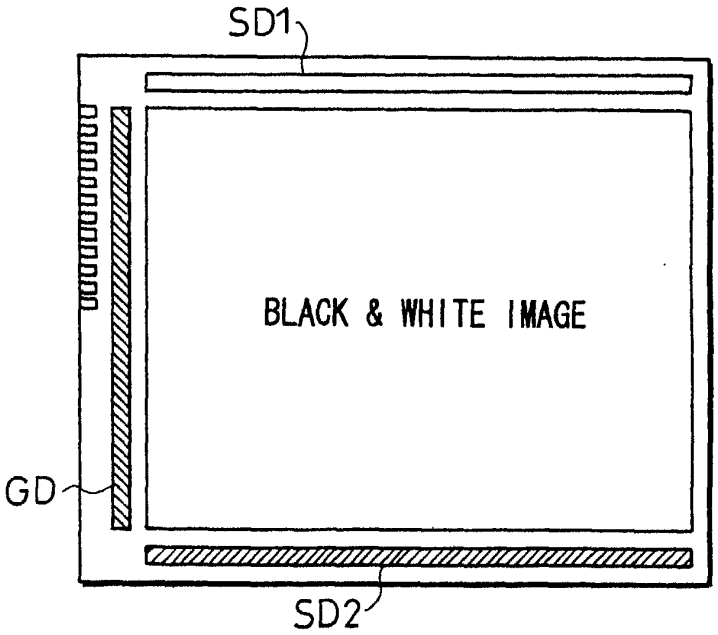

FIG. 54

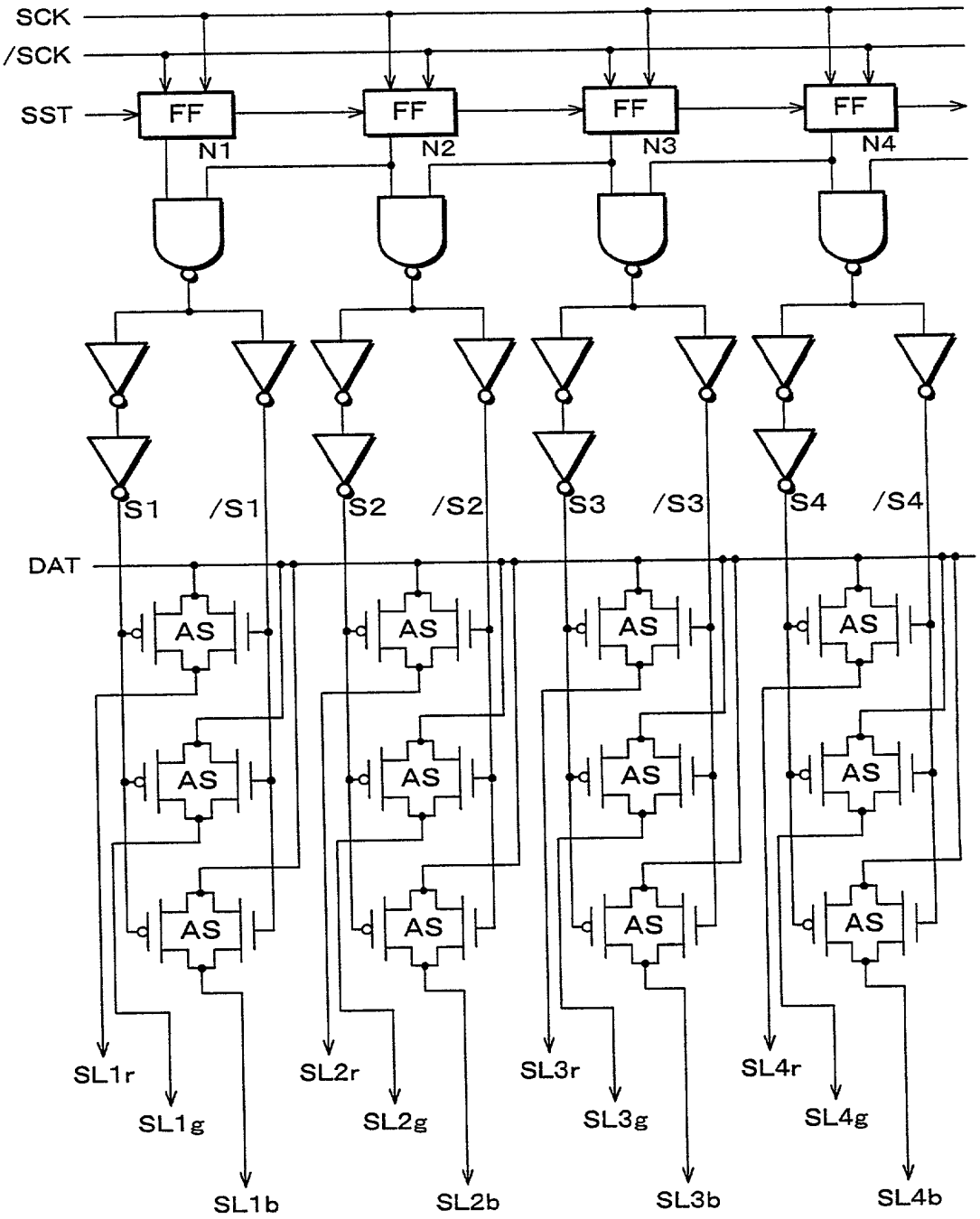
SCK
/SCK
SST
FF
N1
N2
N3
N4
S1
/S1
S2
/S2
S3
/S3
S4
/S4
DAT
AS
SL1r
SL1g
SL1b
SL2r
SL2g
SL2b
SL3r
SL3g
SL3b
SL4r
SL4g
SL4b

FIG. 55(a)

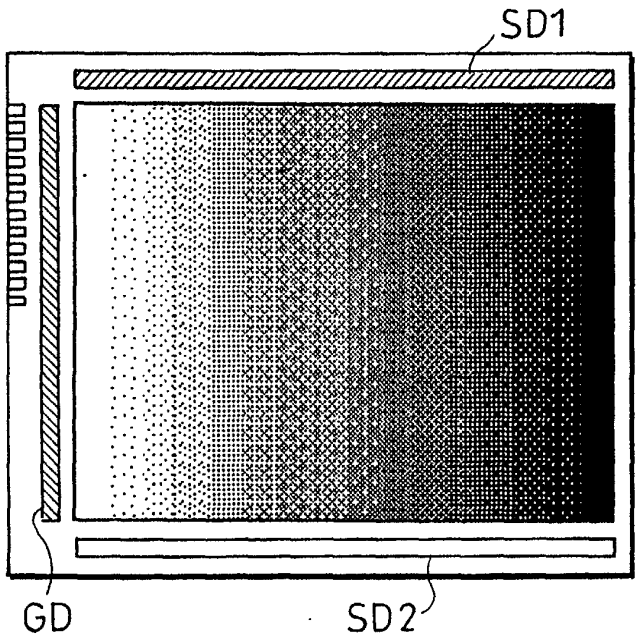

FIG. 55(b)

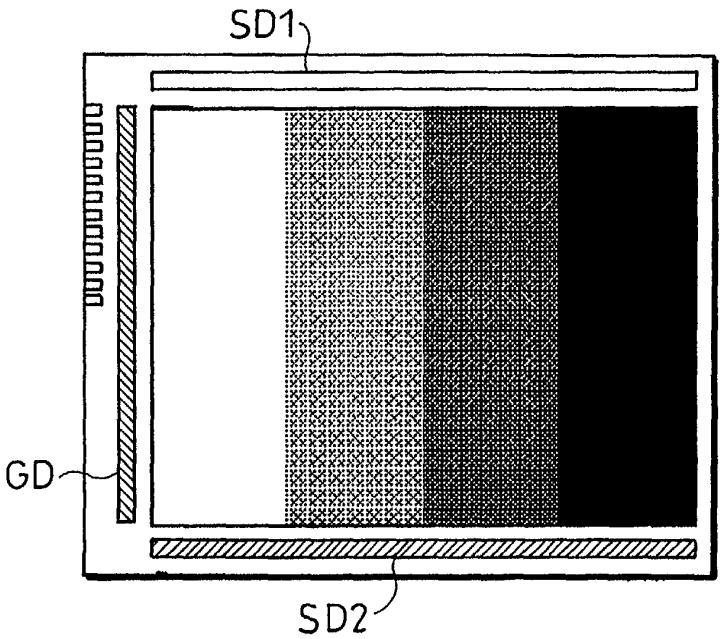

FIG. 56(a)

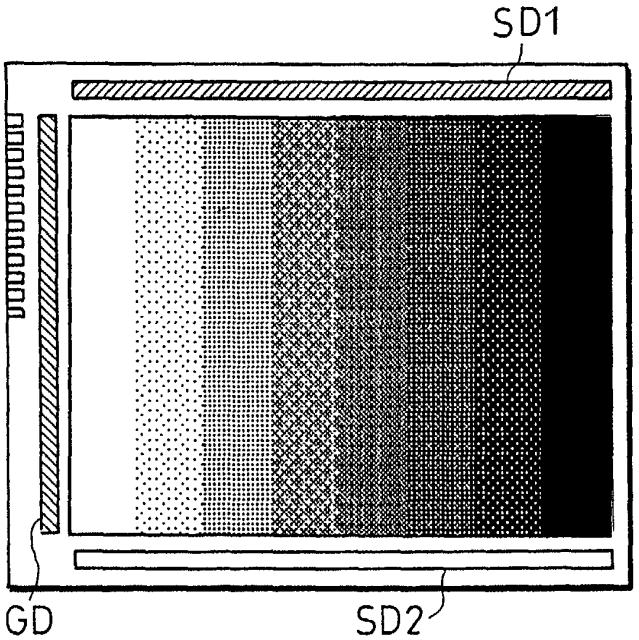

FIG. 56 (b)

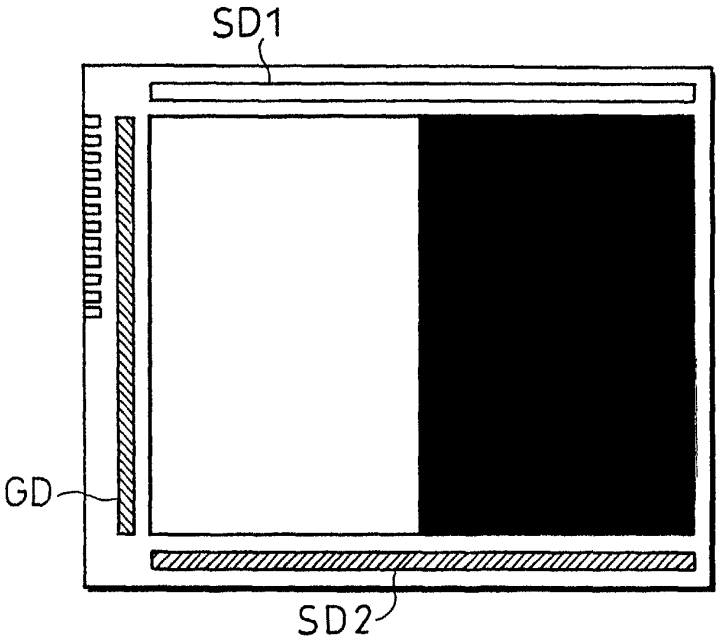

FIG. 57

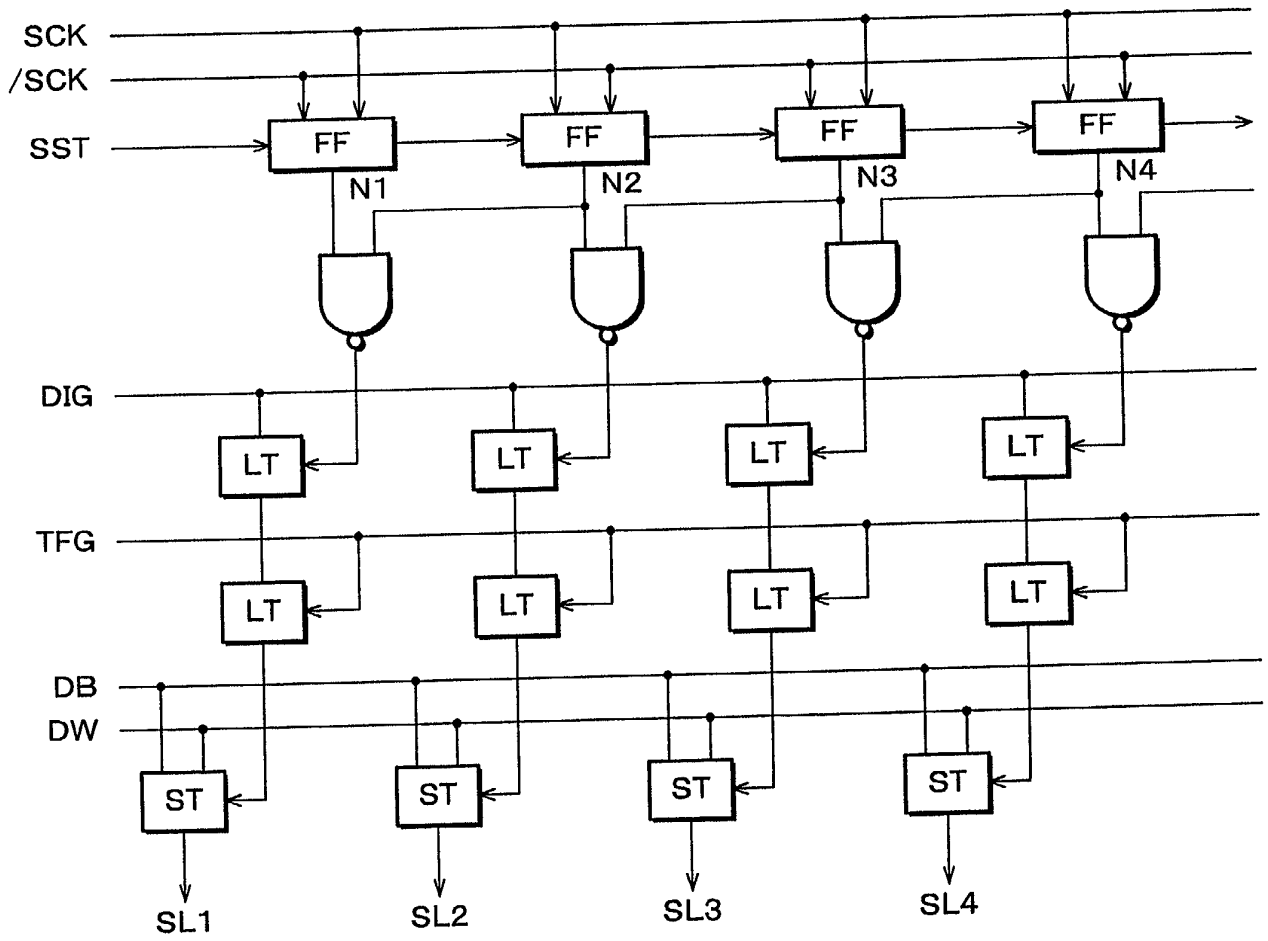
SCK
/SCK
SST
FF
FF
FF
FF
N1
N2
N3
N4
DIG
TFG
LT
DB
DW
ST
SL1
SL2
SL3
SL4

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FIG. 58

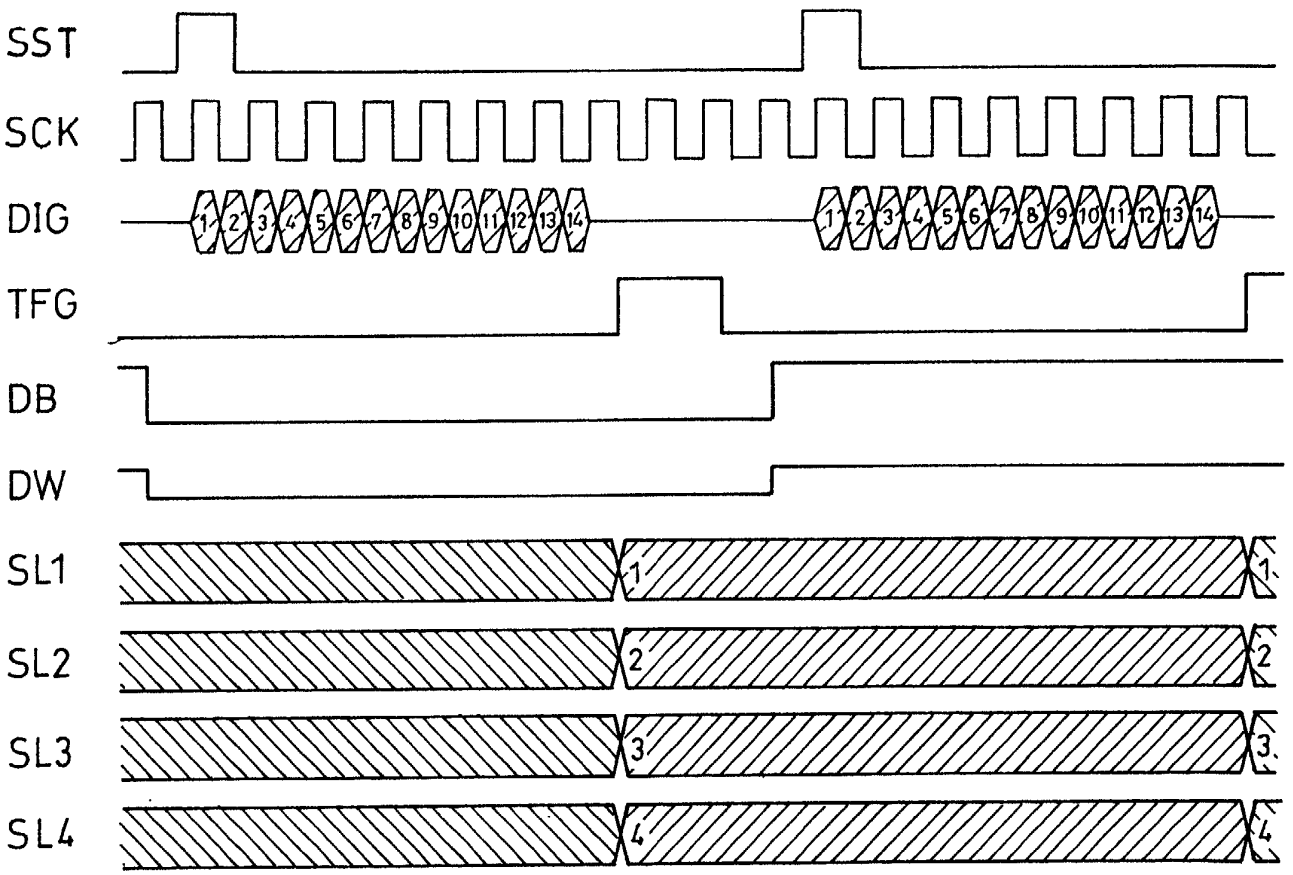
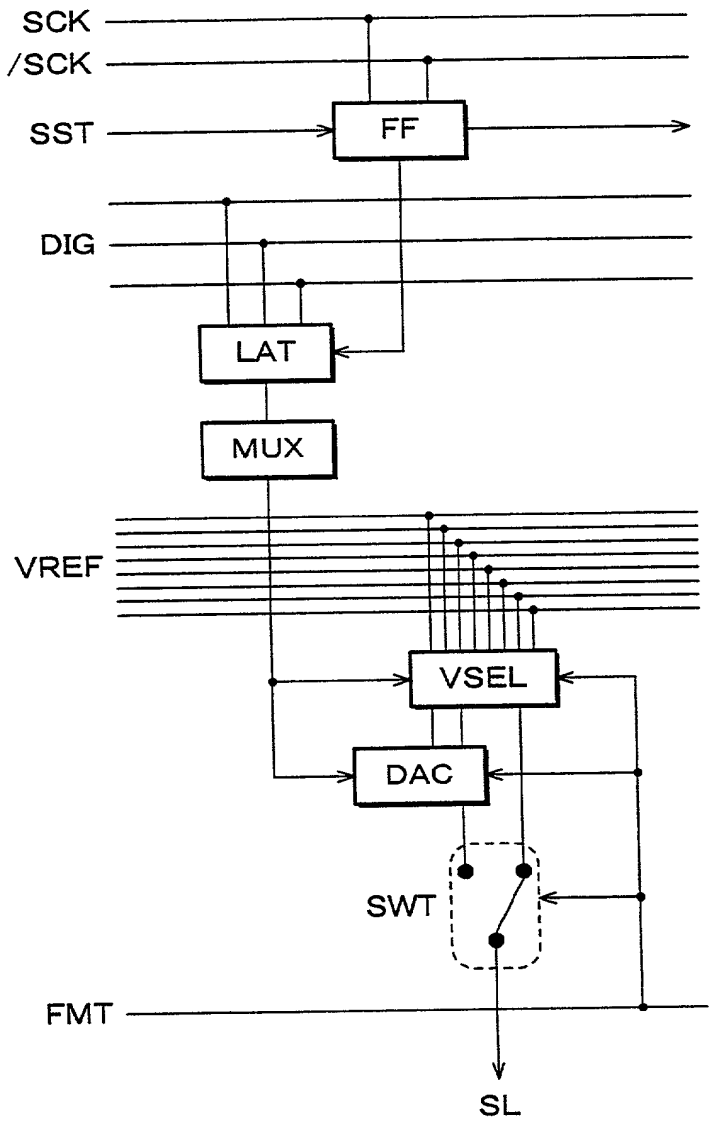


FIG. 59



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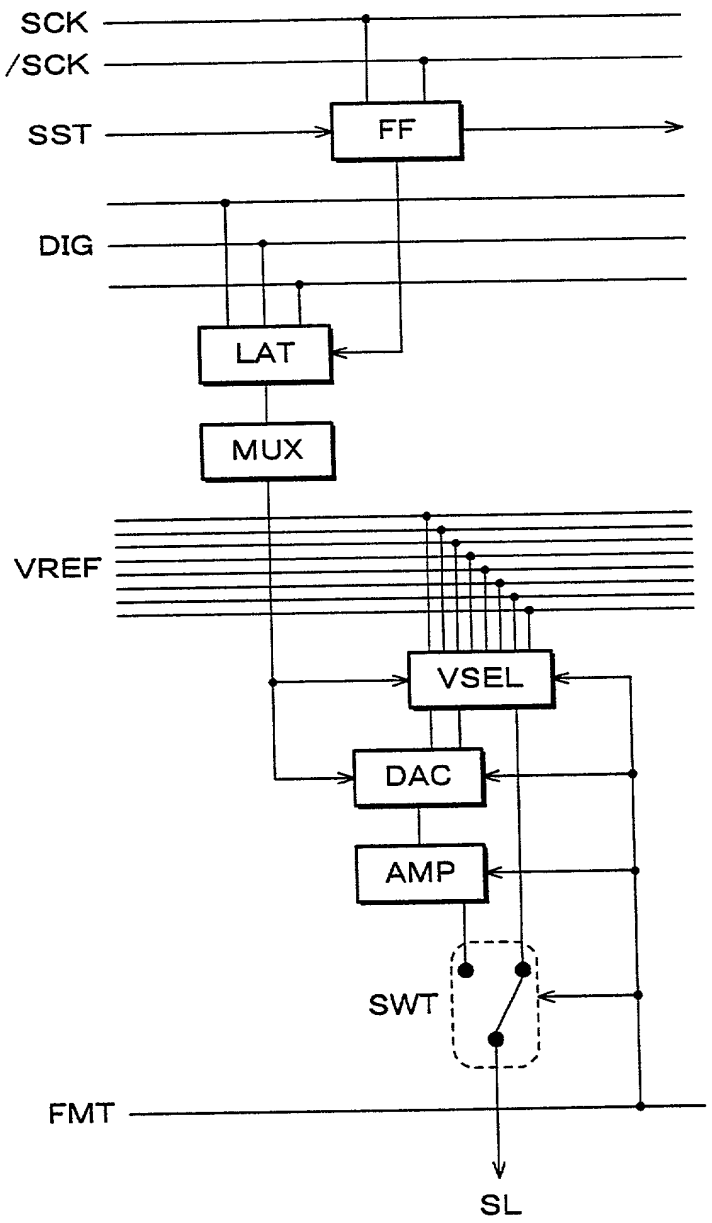

FIG. 61(a)

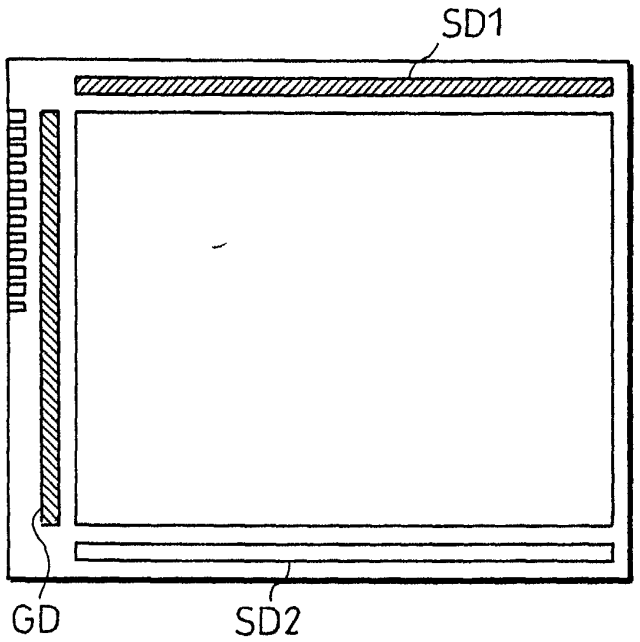

FIG. 61(b)

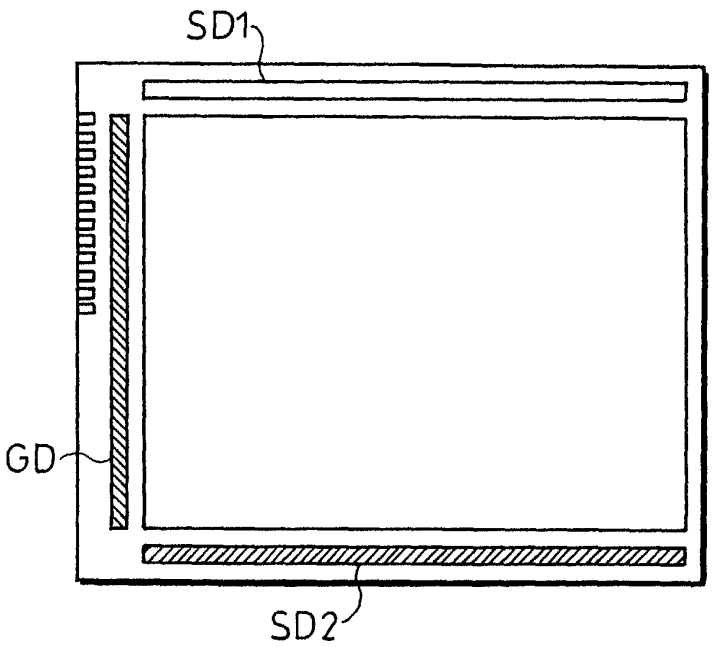

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FIG. 62(a)

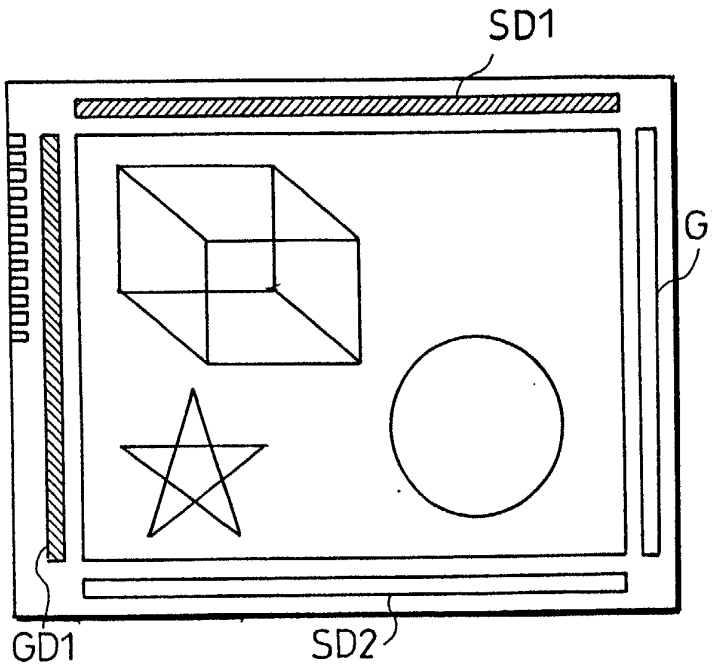

FIG. 62(b)

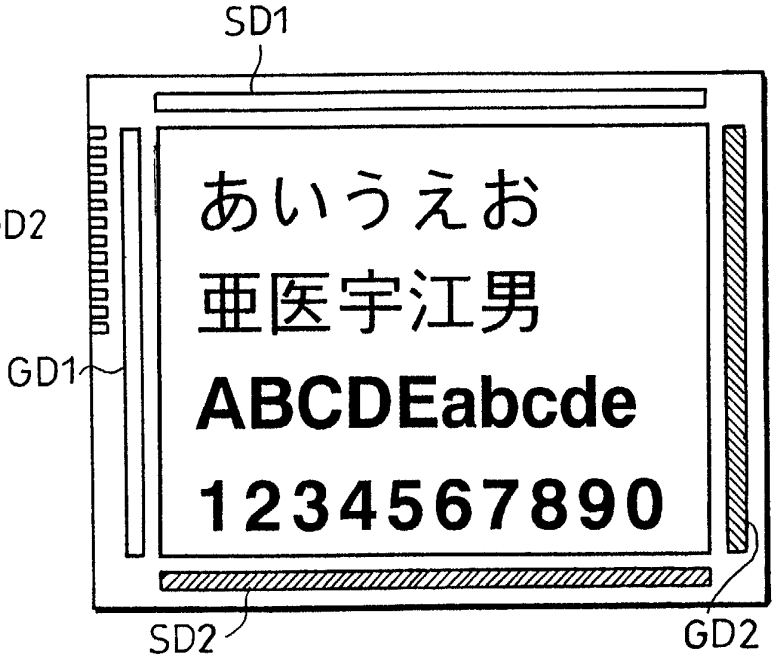

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FIG. 63(a)

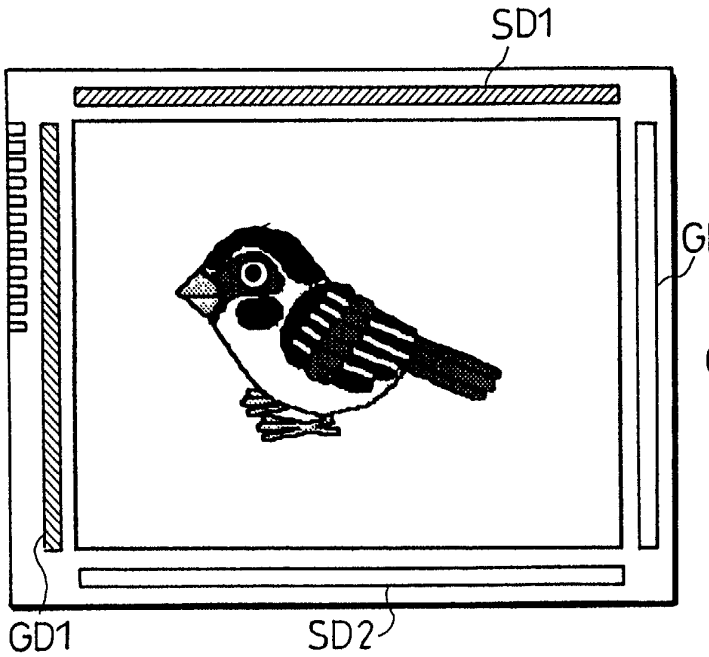

FIG. 63(b)

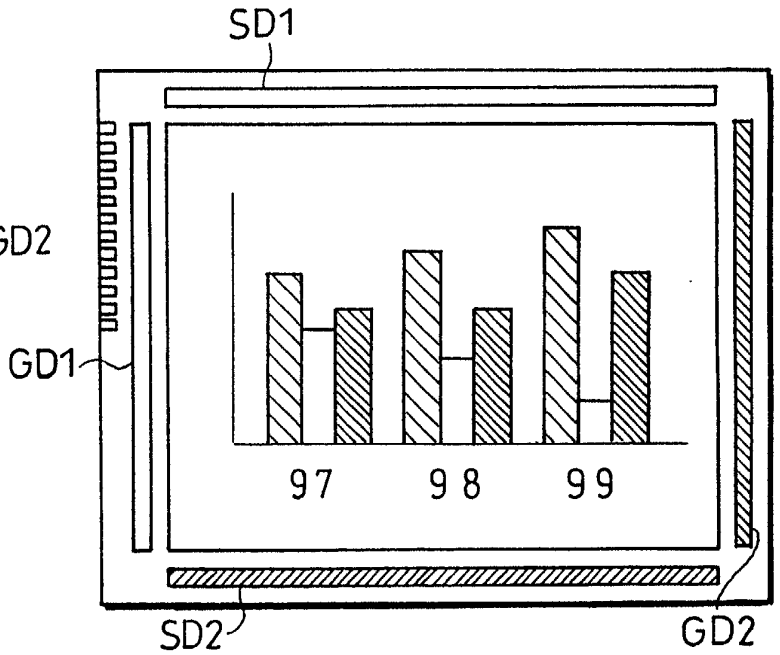

FIG. 64 (a)

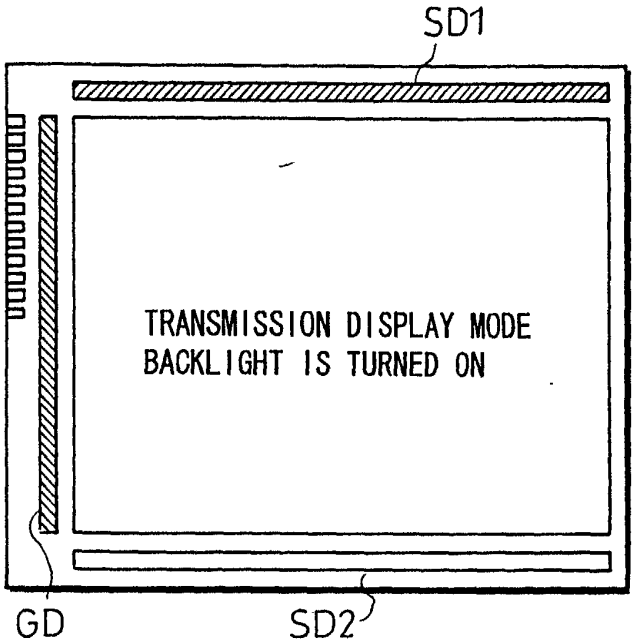

FIG. 64 (b)

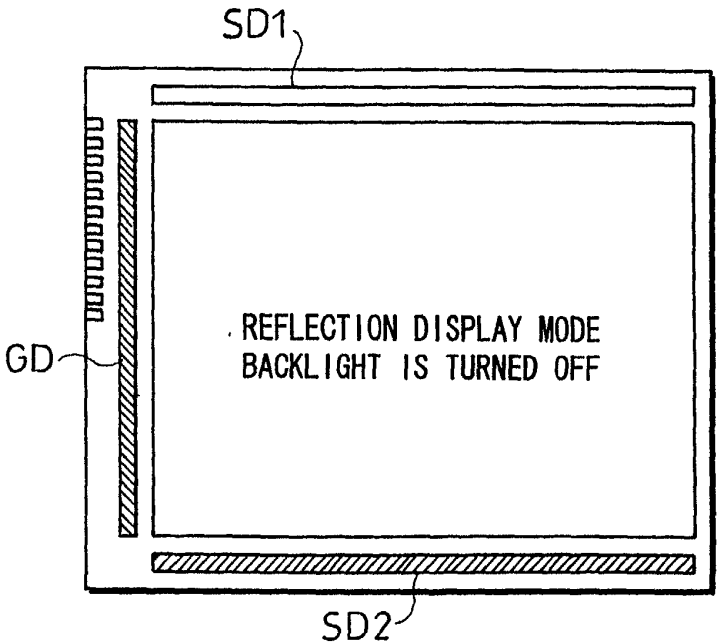

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FIG. 65

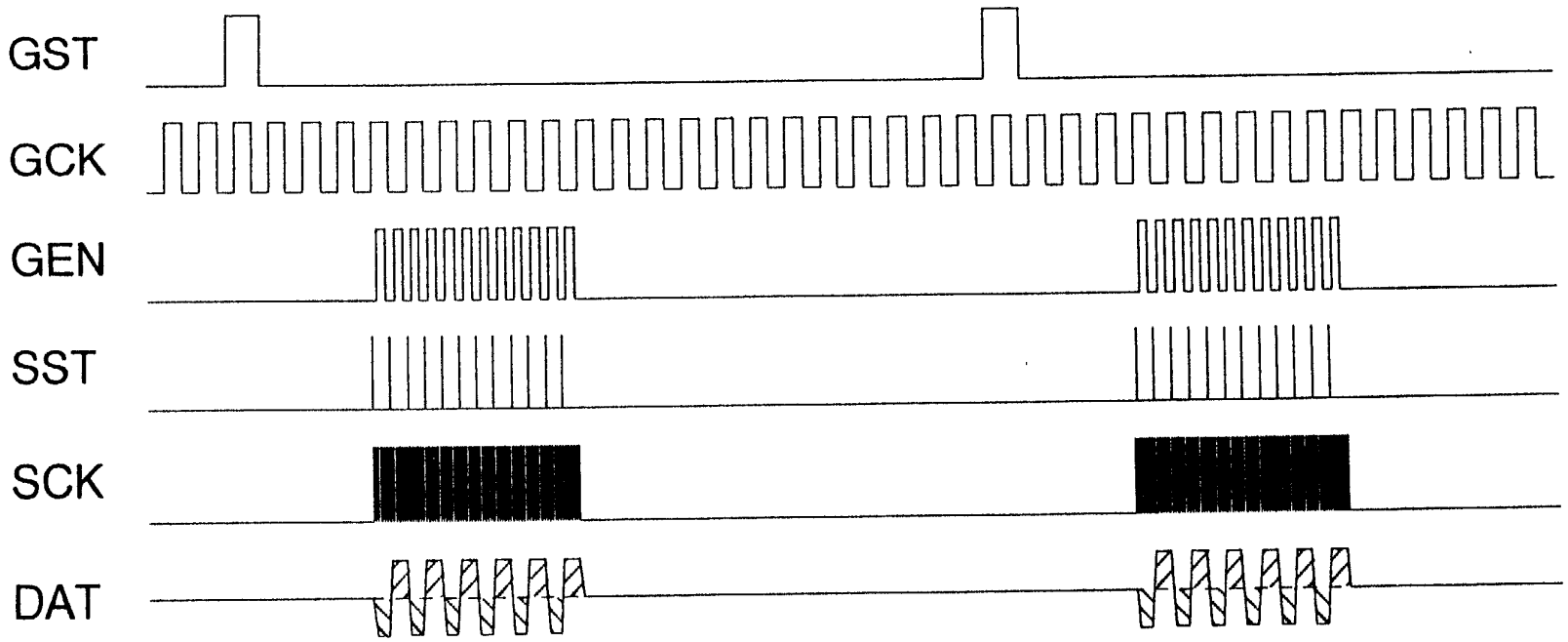

FIG. 66

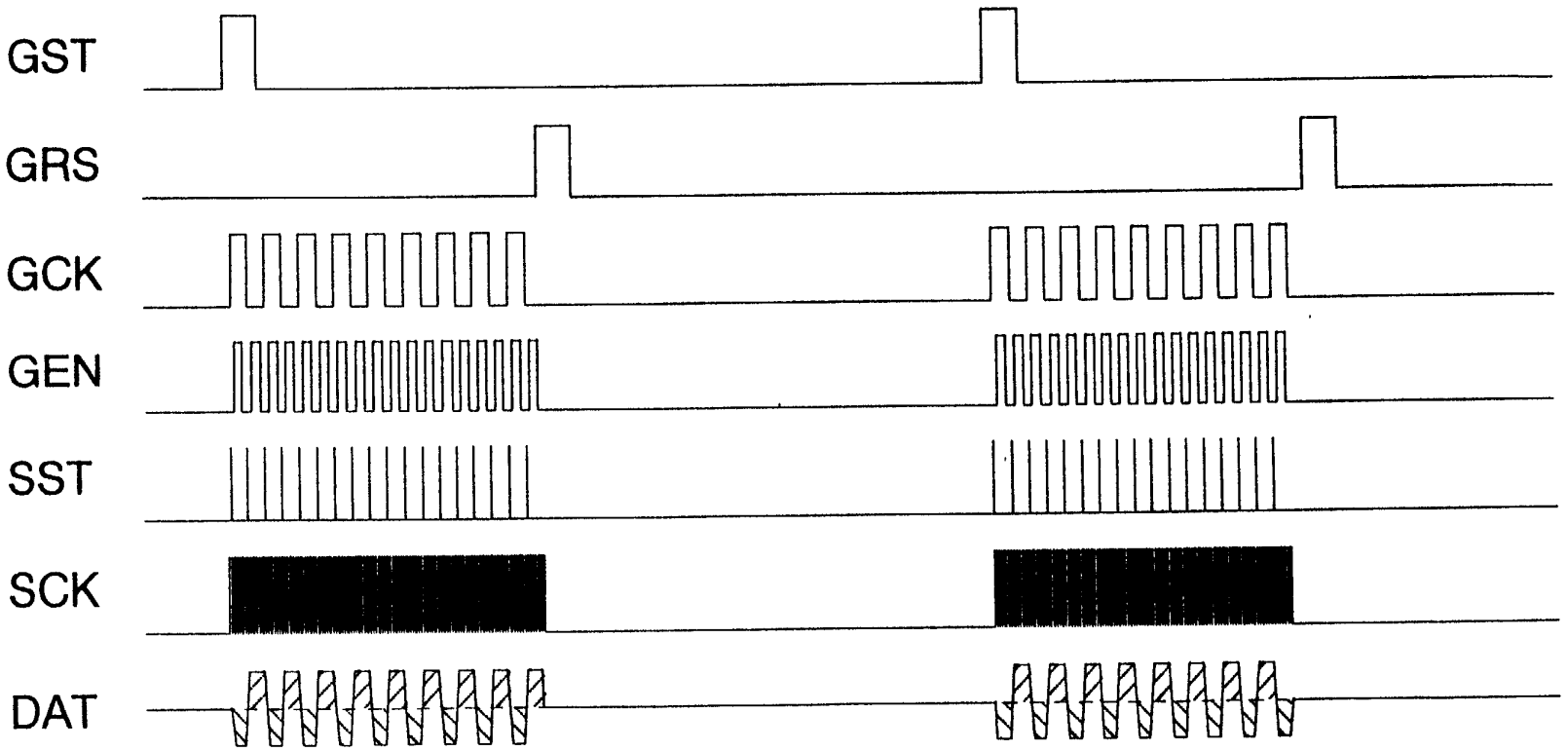

FIG. 67

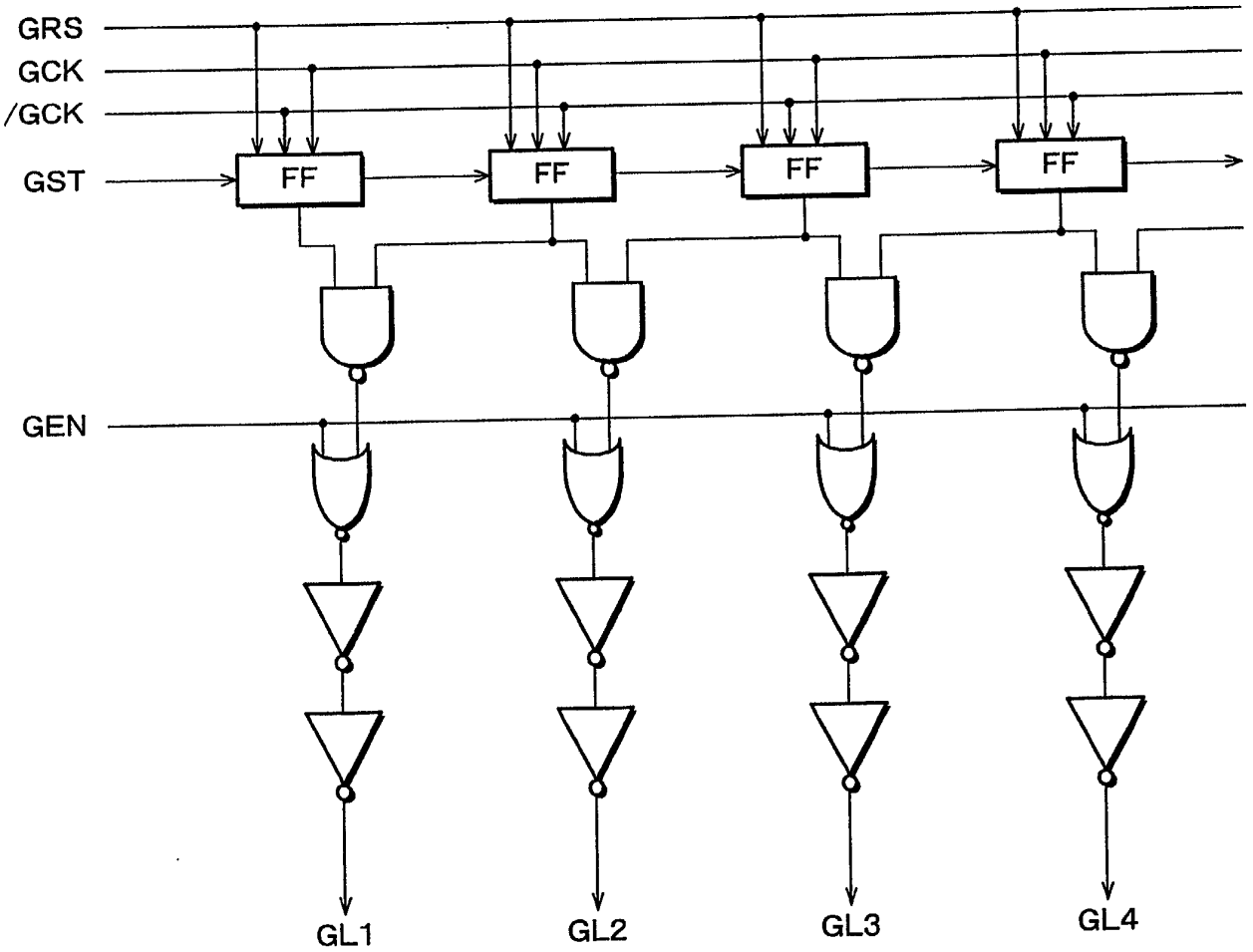

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FIG. 68

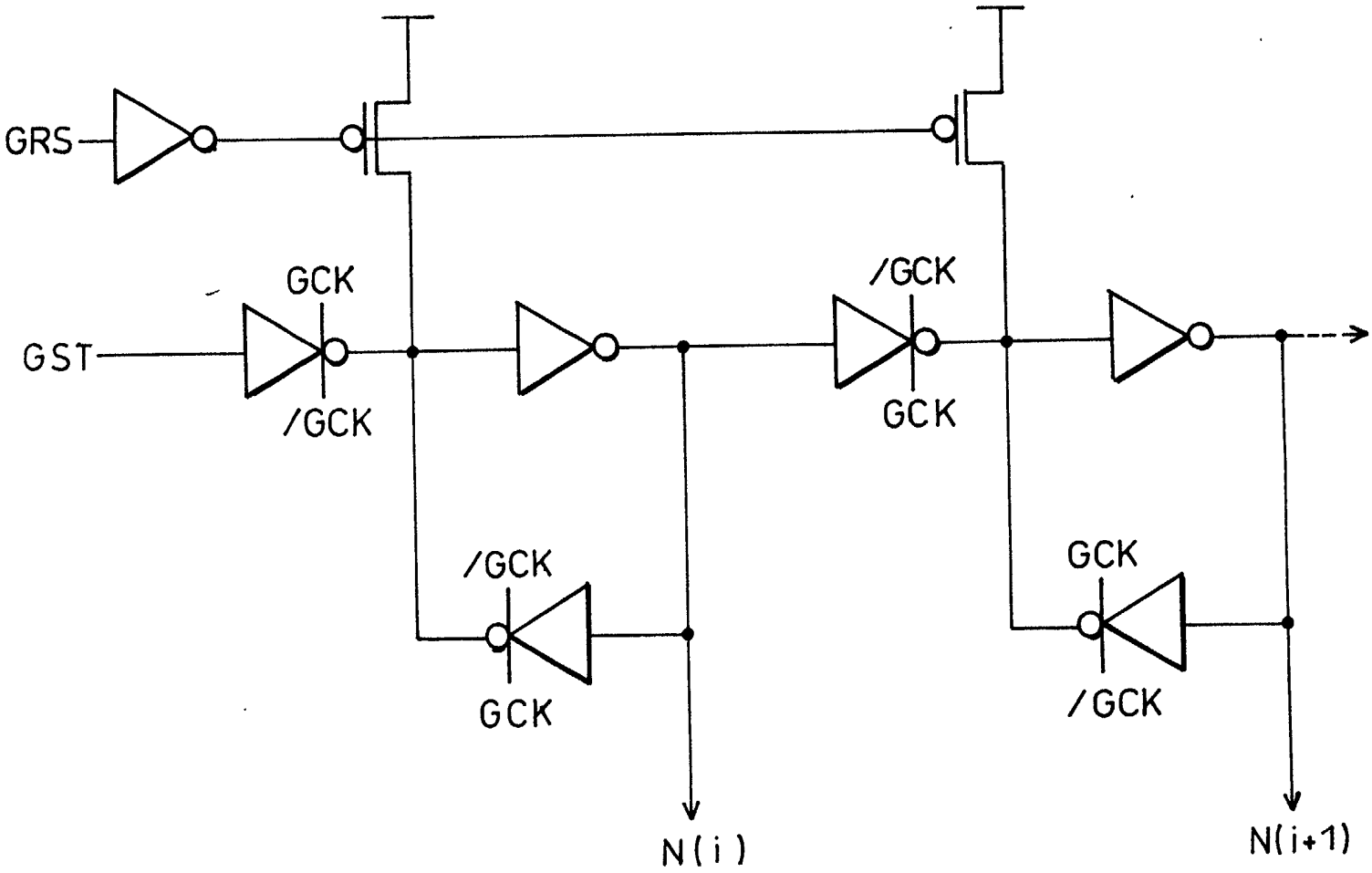

FIG. 69

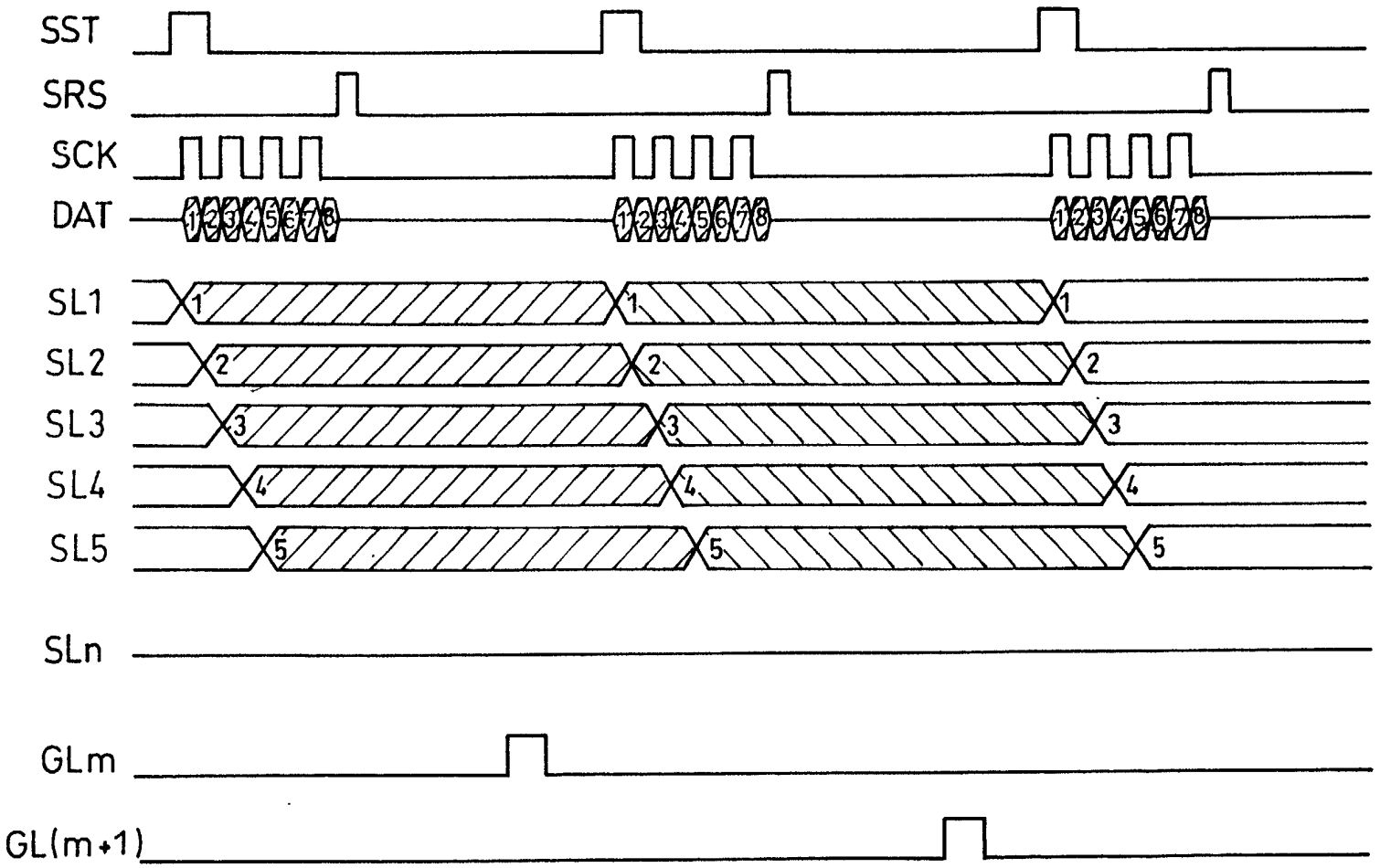

FIG. 70

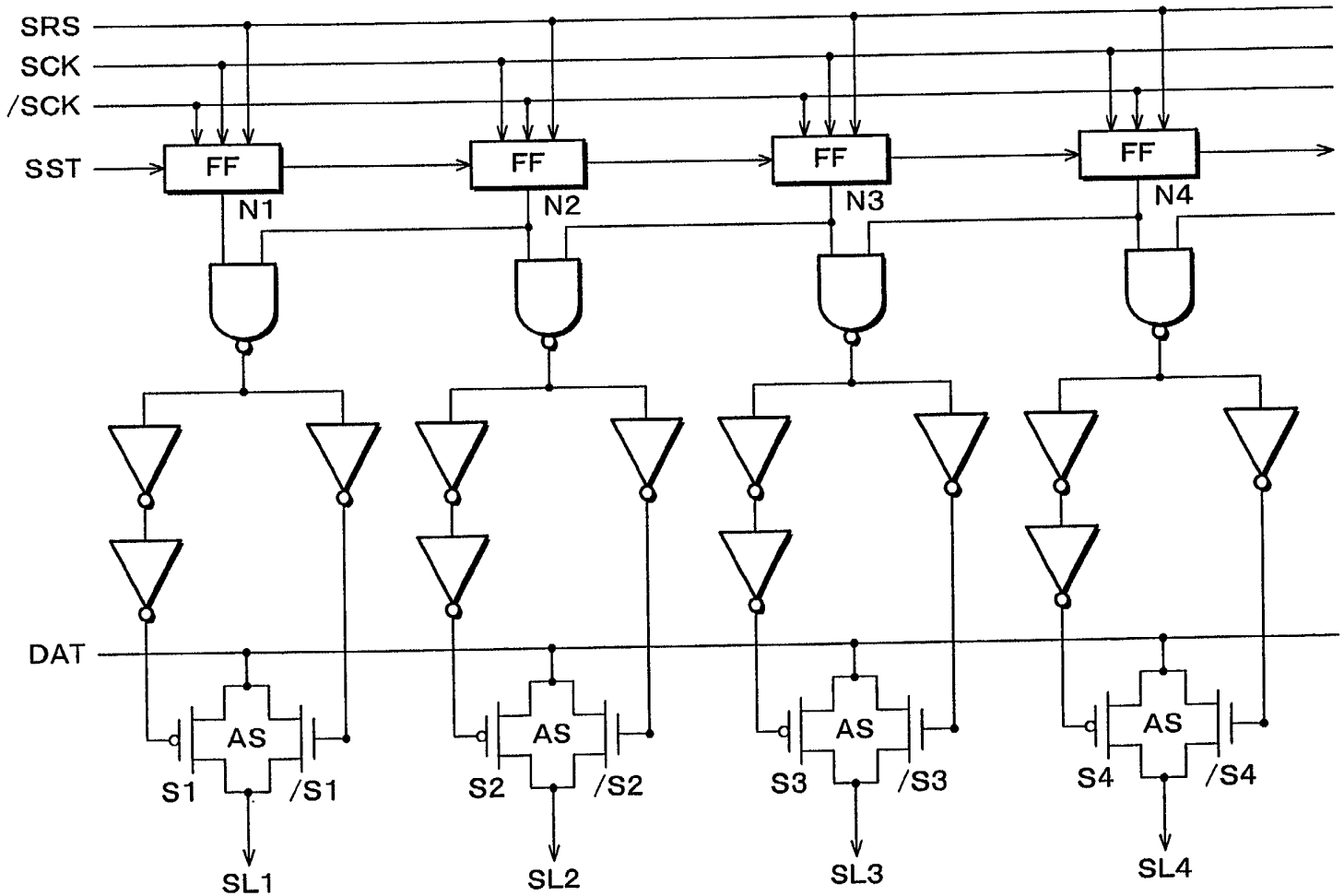
SRS
SCK
/SCK
SST
FF
FF
FF
FF
N1
N2
N3
N4
DAT
AS
AS
AS
AS
S1
/S1
S2
/S2
S3
/S3
S4
/S4
SL1
SL2
SL3
SL4

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FIG. 71

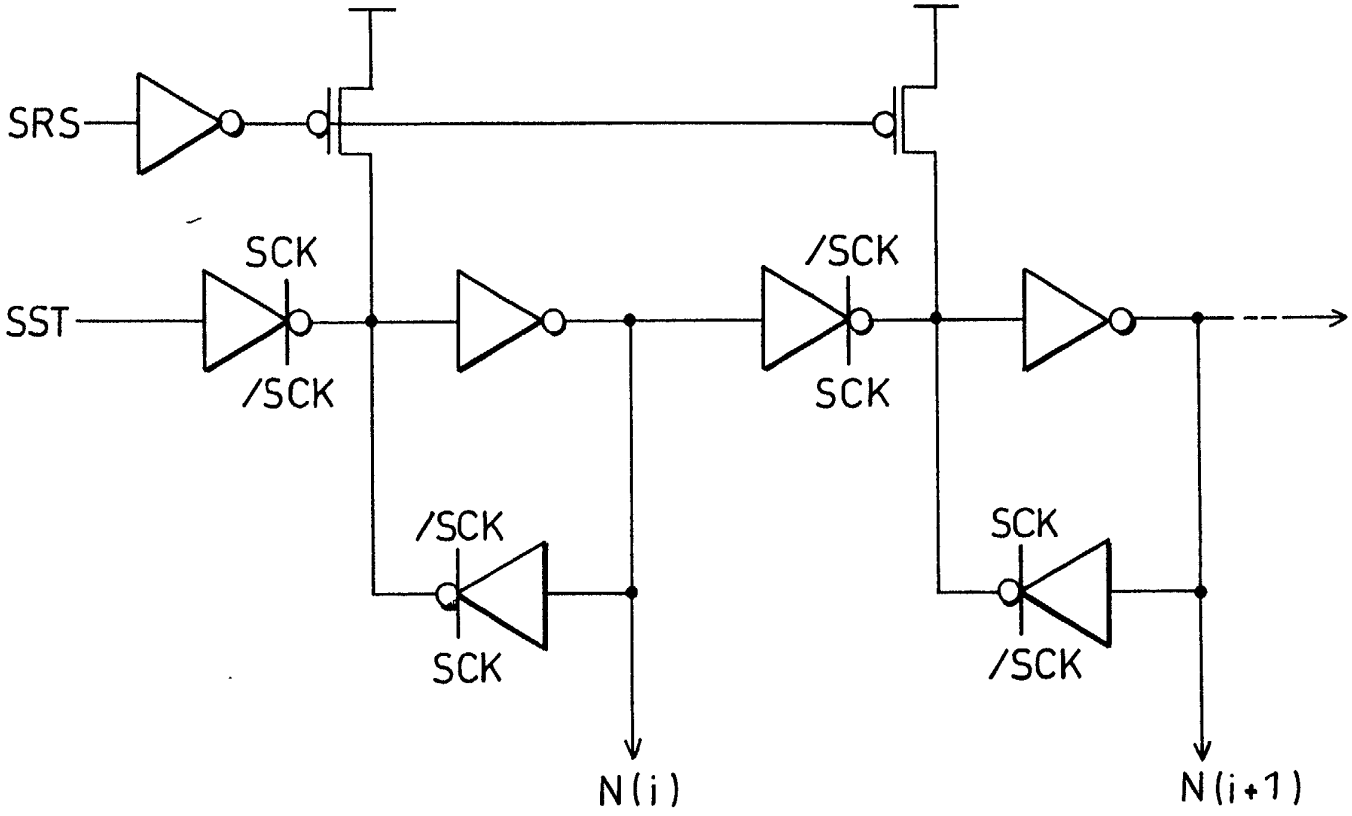


FIG. 72

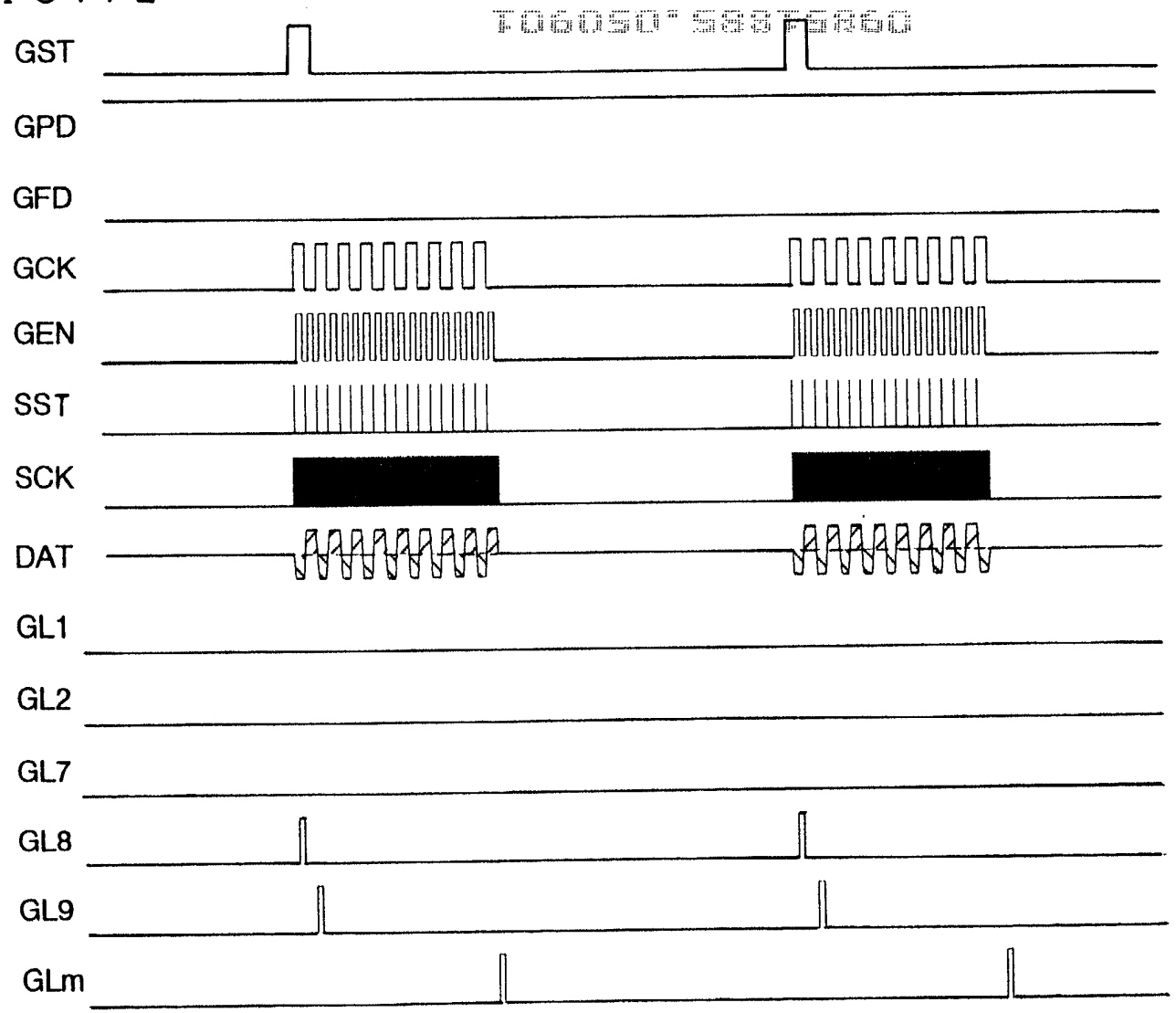
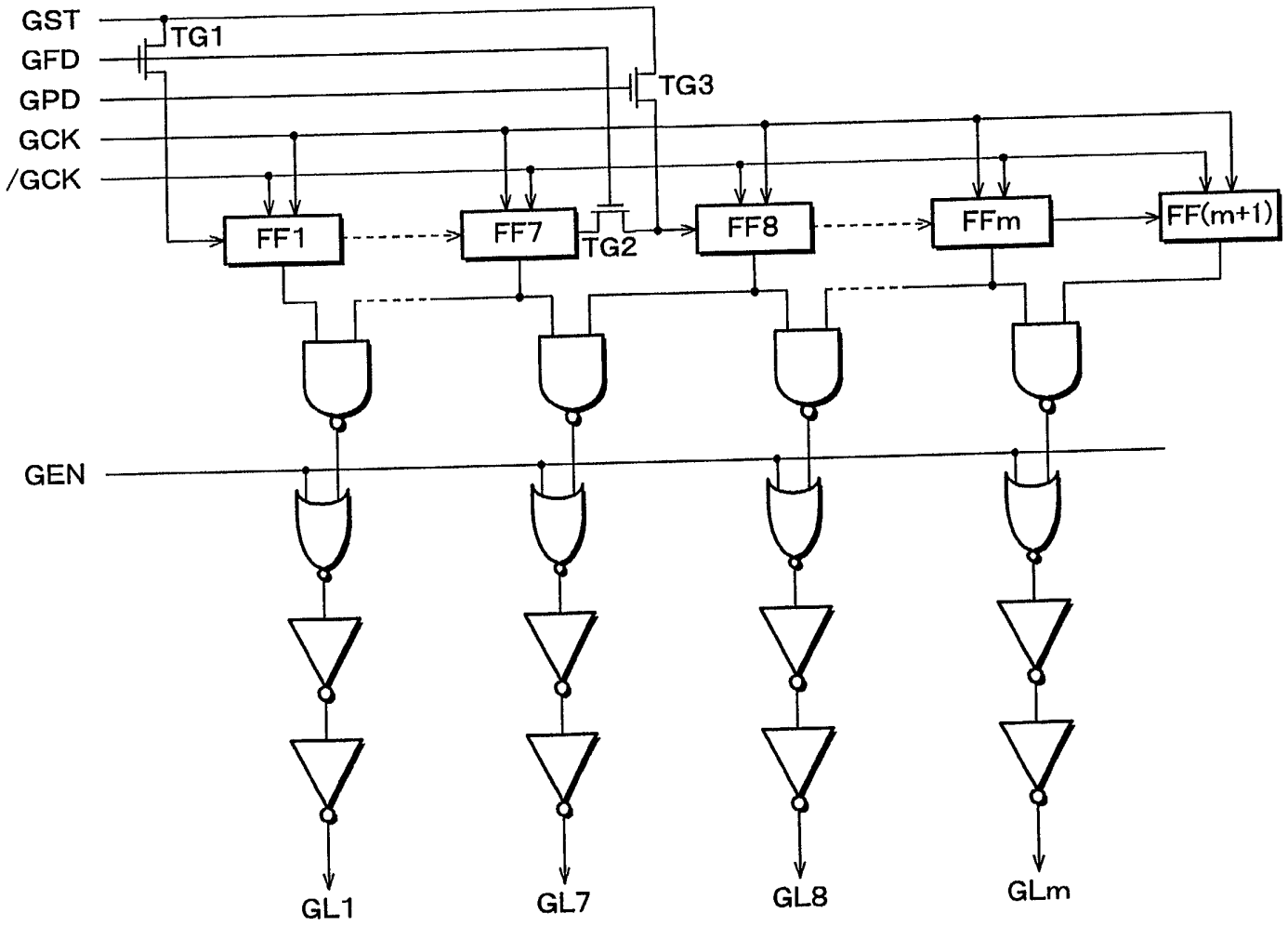


FIG. 73


GST
GFD
GPD
GCK
/GCK
TG1
TG3
TG2
FF1
FF7
FF8
FFm
FF(m+1)
GEN
GL1
GL7
GL8
GLm

JP06030"5887580

FIG. 74

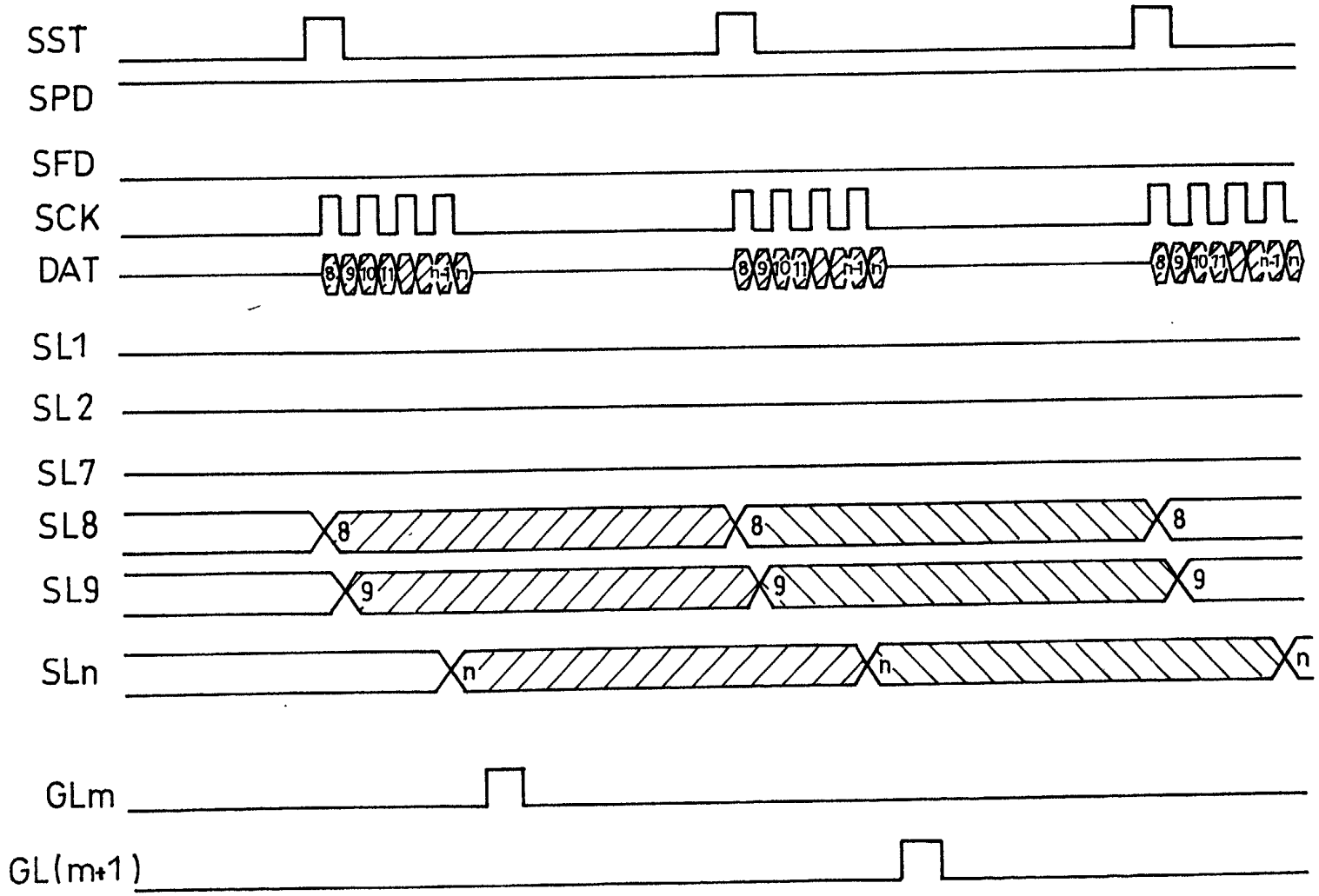


FIG. 75

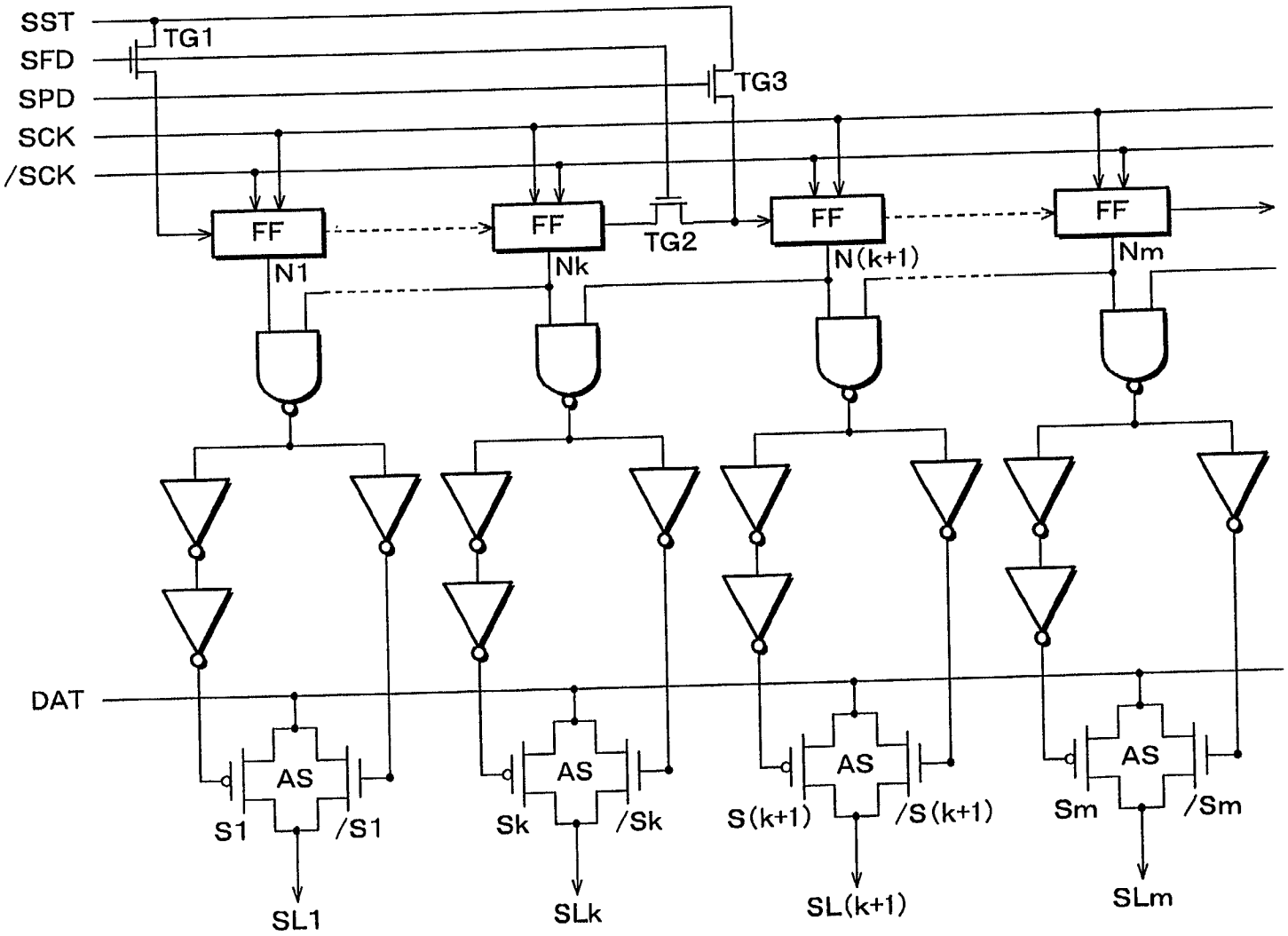

SST
SFD
SPD
SCK
/SCK
TG1
TG3
TG2
FF
FF
FF
FF
N1
Nk
N(k+1)
Nm
DAT
AS
AS
AS
AS
S1
/S1
Sk
/Sk
S(k+1)
/S(k+1)
Sm
/Sm
SL1
SLk
SL(k+1)
SLm

FIG. 76

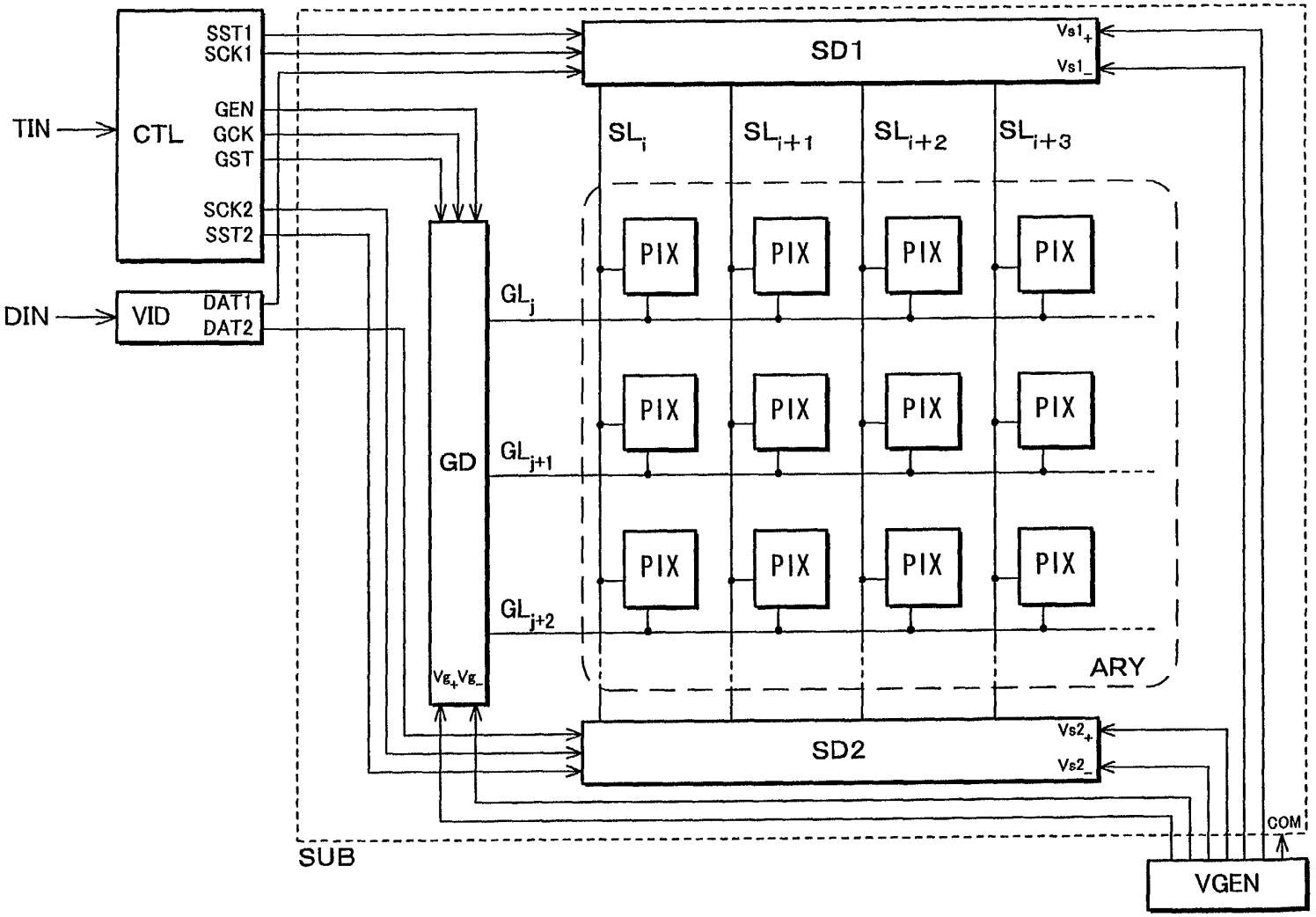

SST1
SCK1
GEN
GCK
GST
SCK2
SST2
TIN
CTL
DIN
VID
DAT1
DAT2
SD1
Vs1+
Vs1_
SLi
SLi+1
SLi+2
SLi+3
PIX
GLj
GLj+1
GLj+2
GD
Vg+Vg_
ARY
SD2
Vs2+
Vs2_
COM
SUB
VGEN

FIG. 77

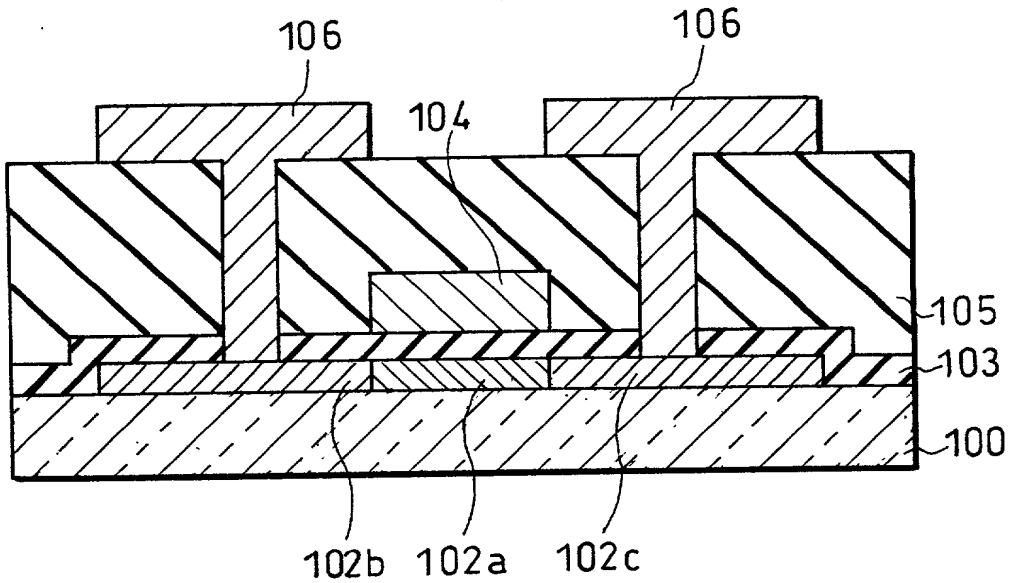


FIG. 78 (a)

FIG. 78 (b)

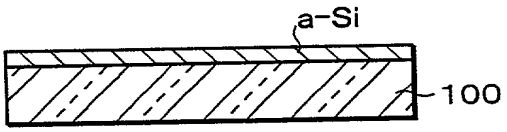


FIG. 78 (c)

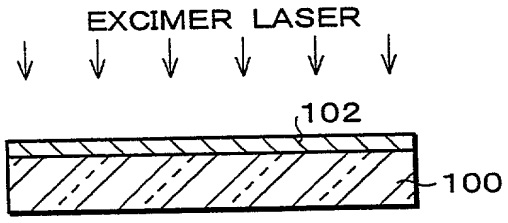


FIG. 78 (d)

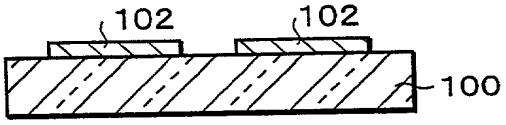


FIG. 78 (e)

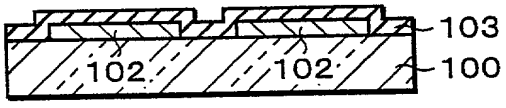


FIG. 78 (f)

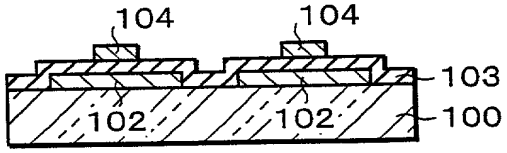


FIG. 78 (g)

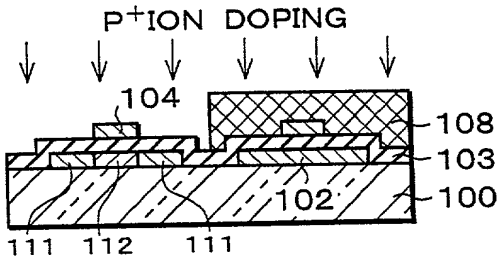


FIG. 78 (h)

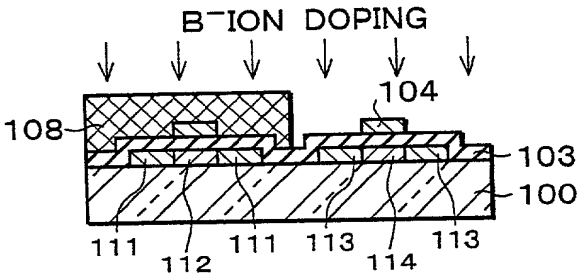


FIG. 78 (i)

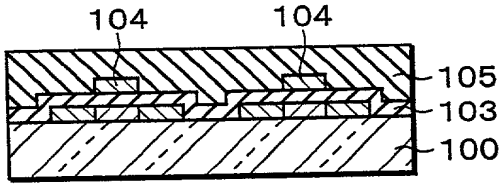


FIG. 78 (j)

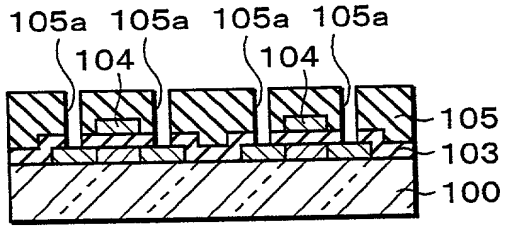


FIG. 78 (k)

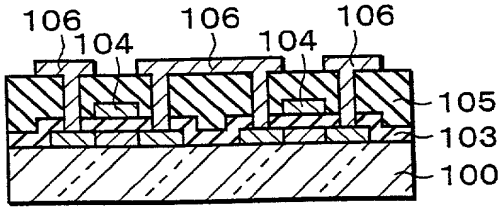


FIG. 79

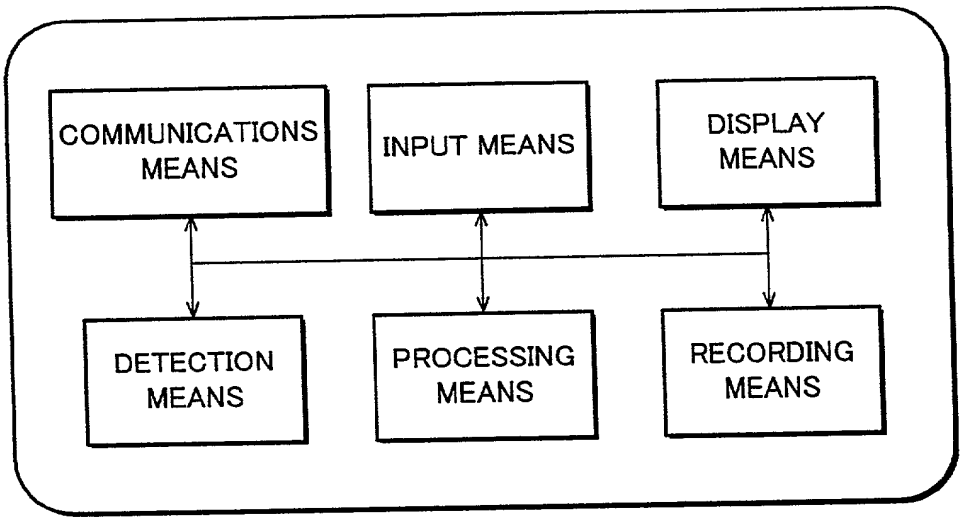

COMMUNICATIONS MEANS
INPUT MEANS
DISPLAY MEANS
DETECTION MEANS
PROCESSING MEANS
RECORDING MEANS

FIG. 80 (a)

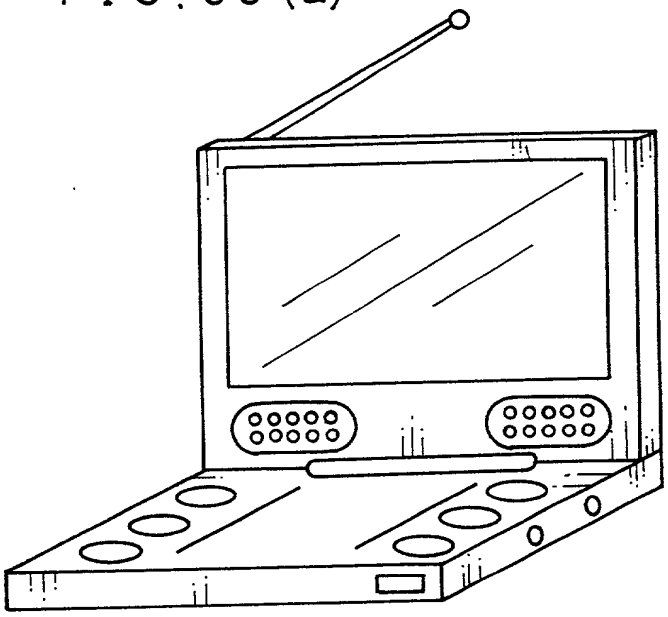


FIG. 80(b)

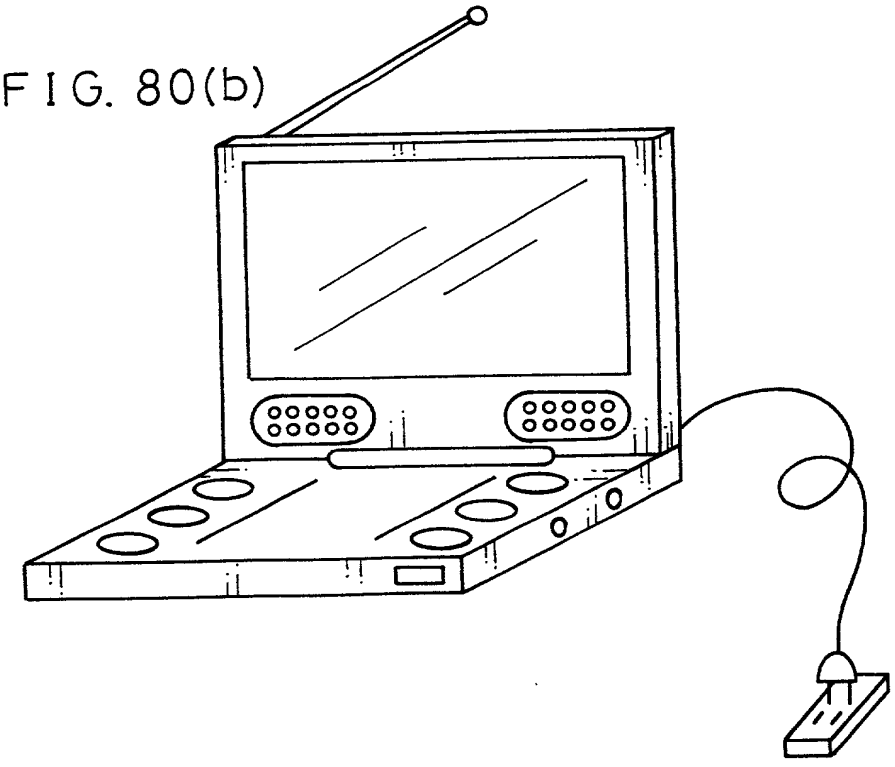


FIG. 81(a)

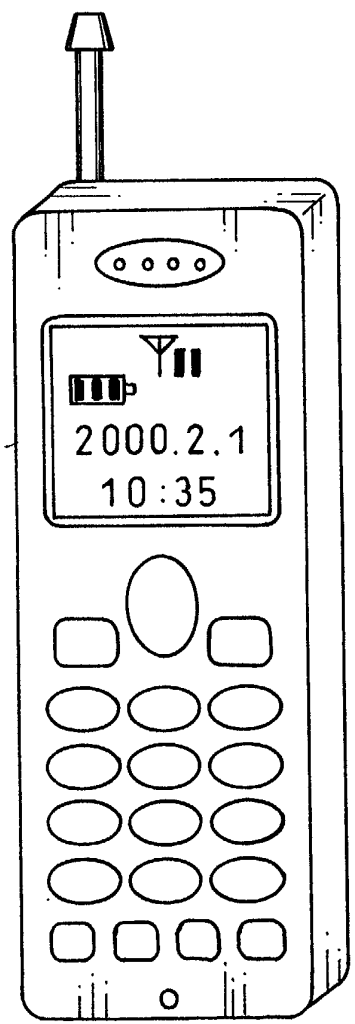


FIG. 81(b)

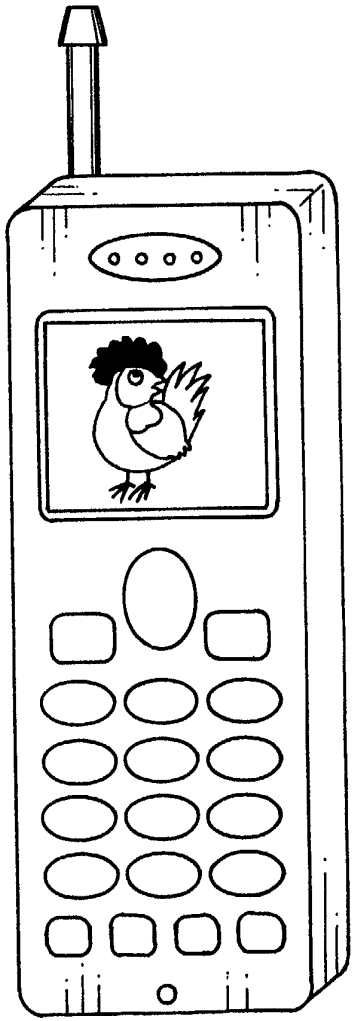


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FIG. 82

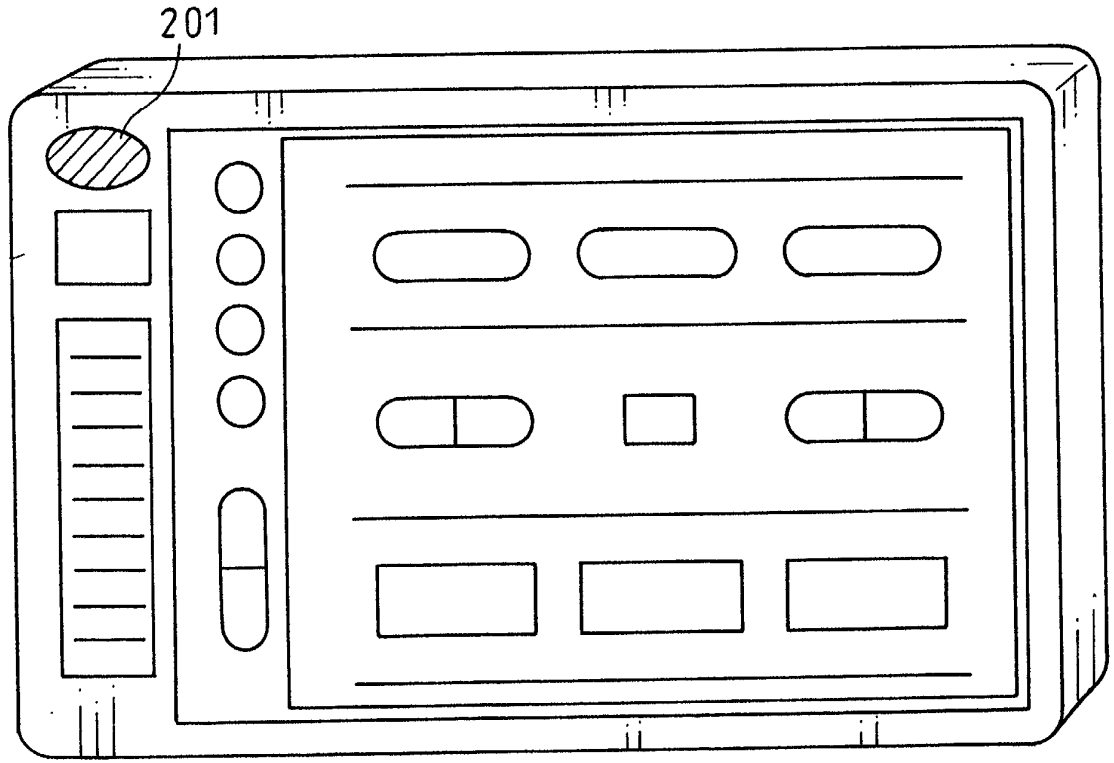

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FIG. 83

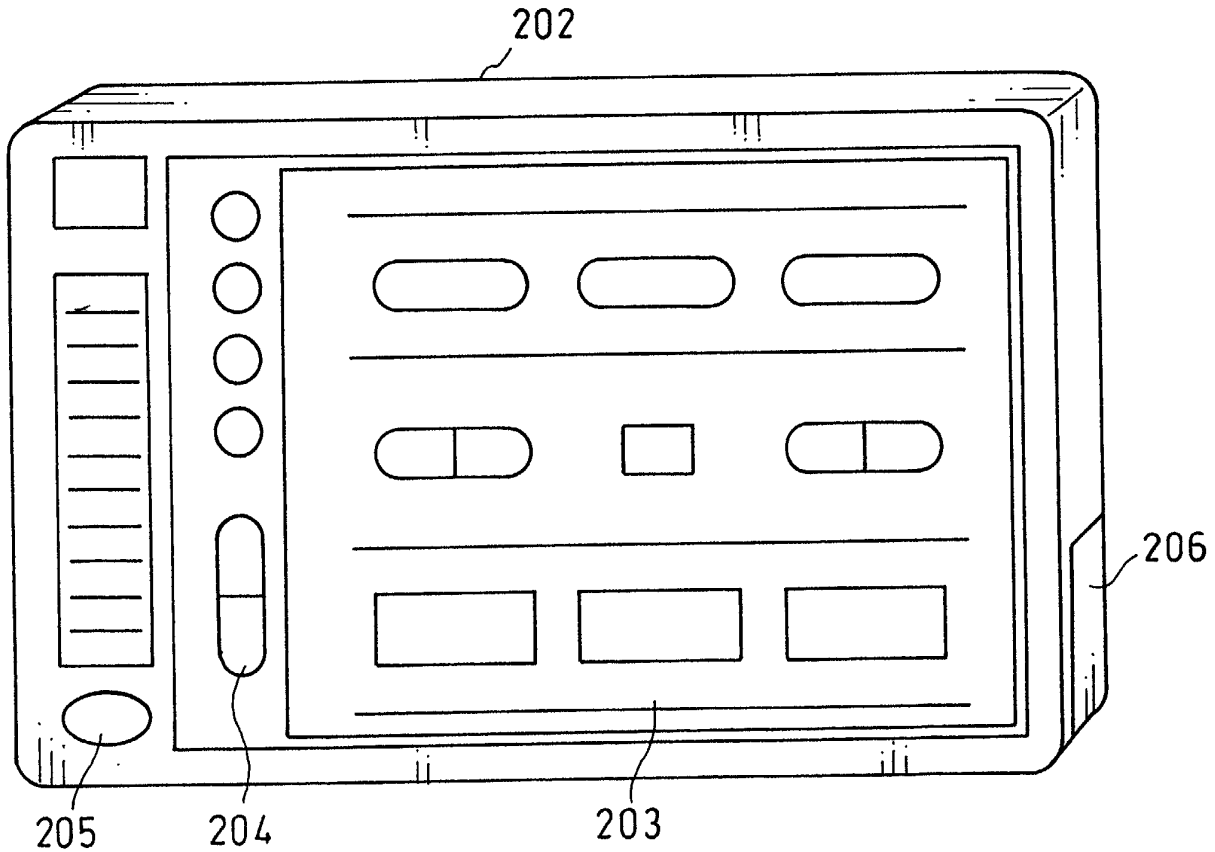

FIG. 84

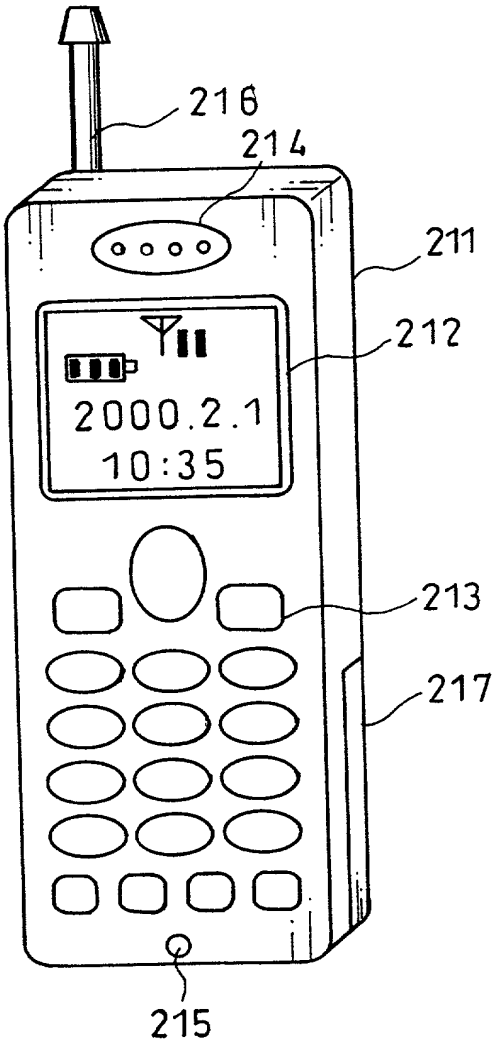

FIG. 85

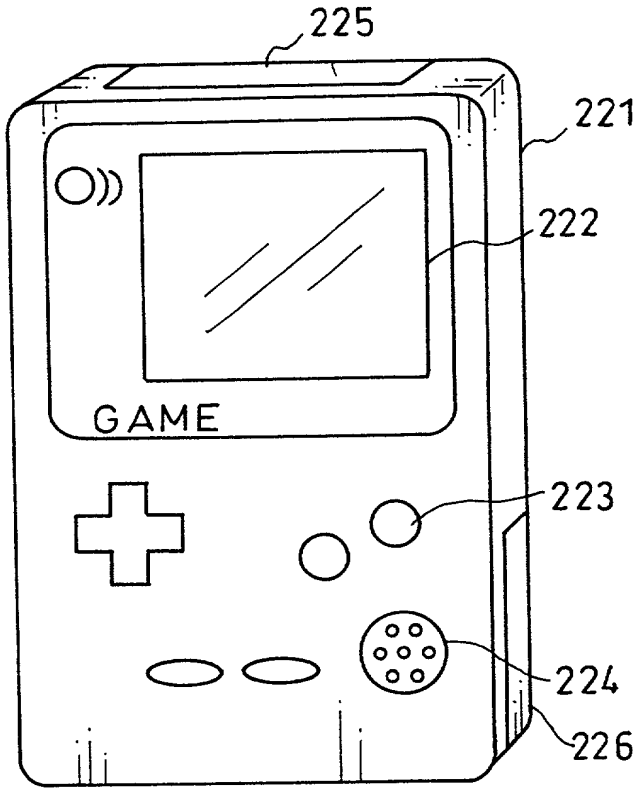

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FIG. 86(a)

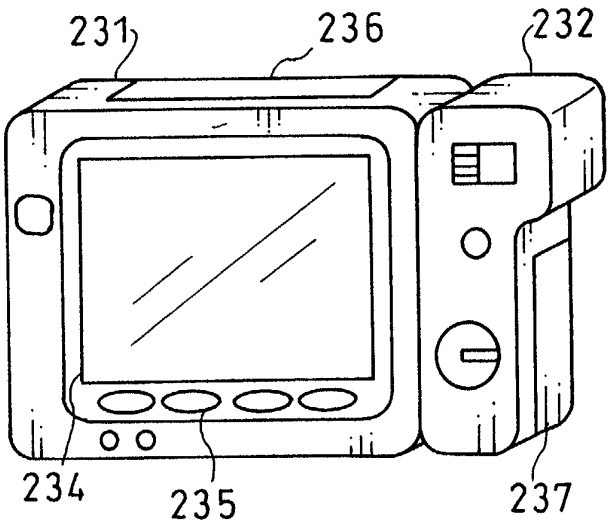

FIG. 86(b)

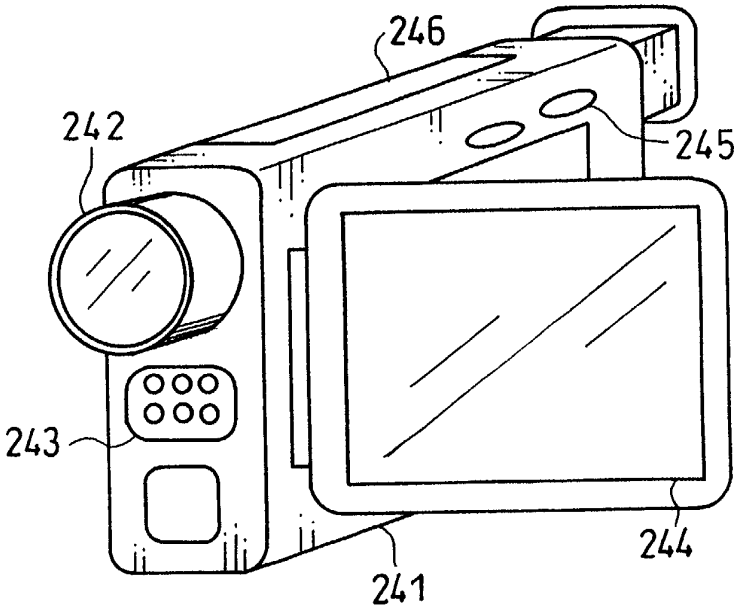

FIG. 87

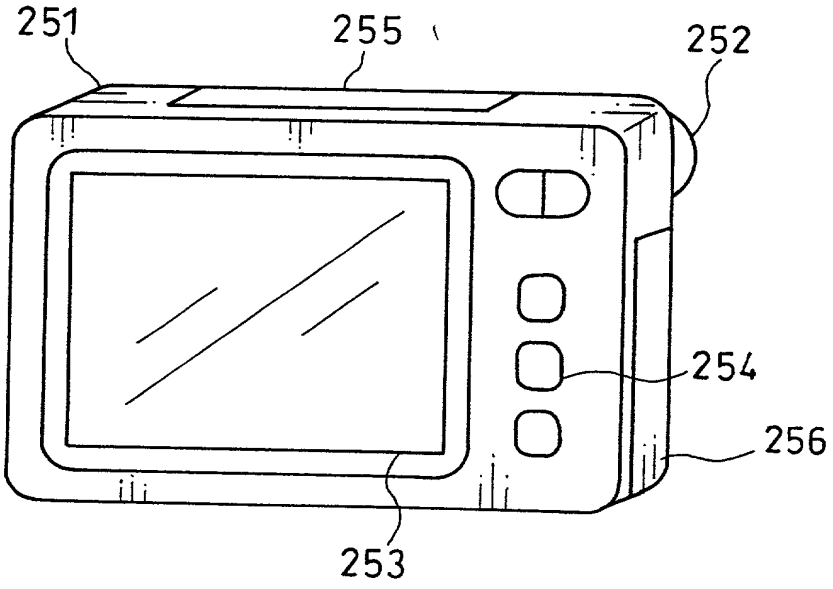

FIG. 88

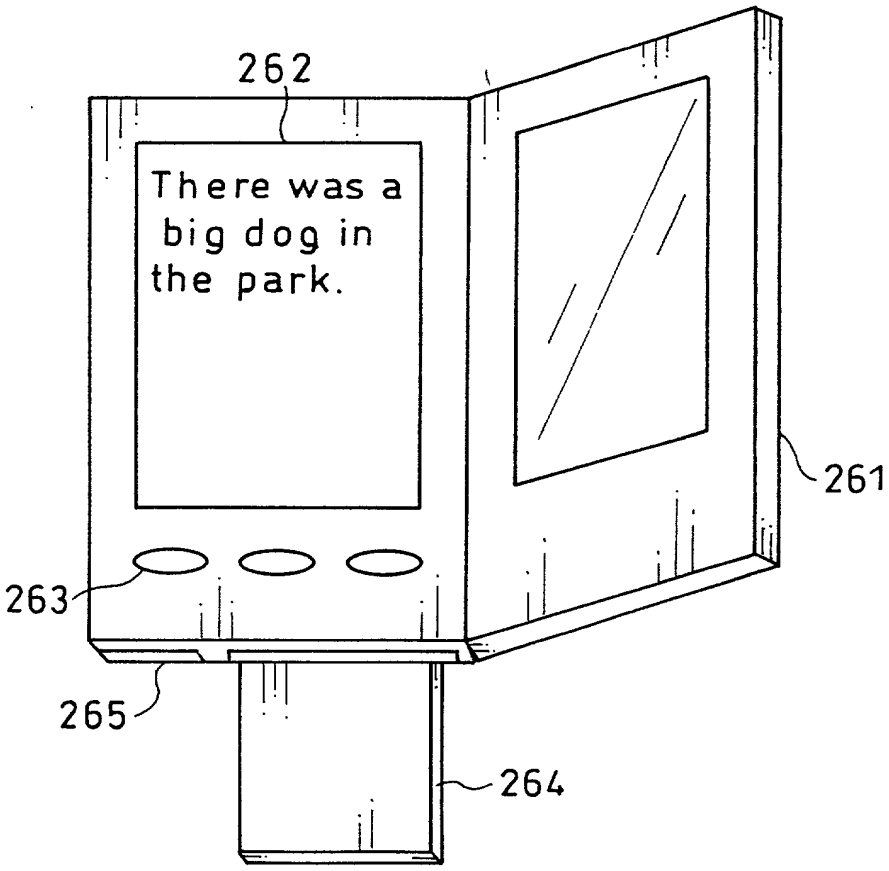

FIG. 89

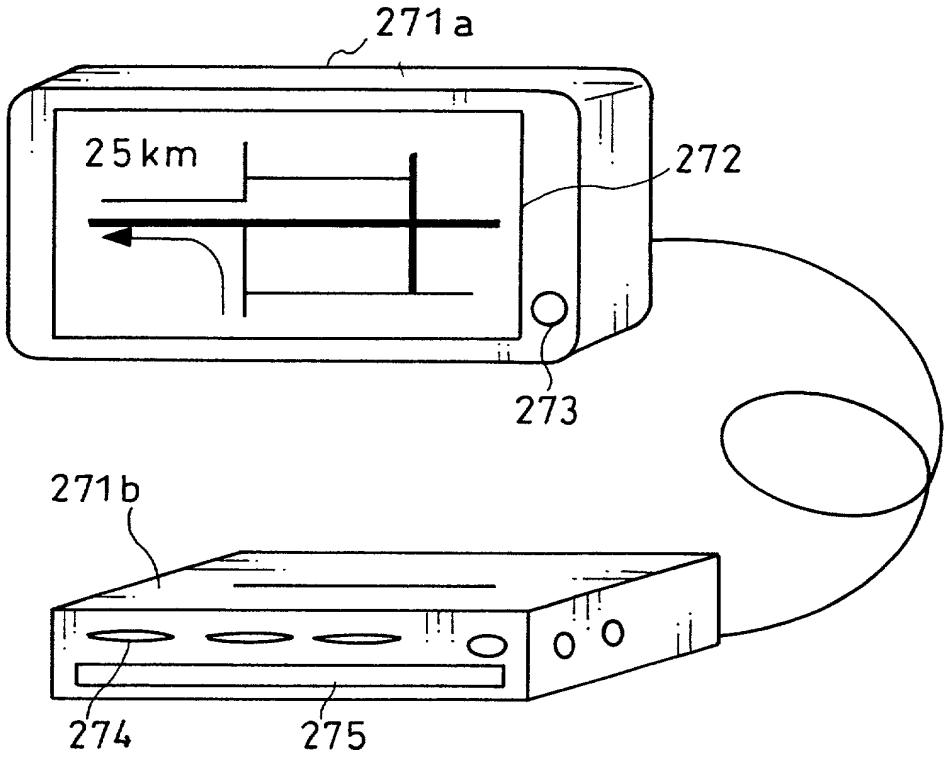

FIG. 90

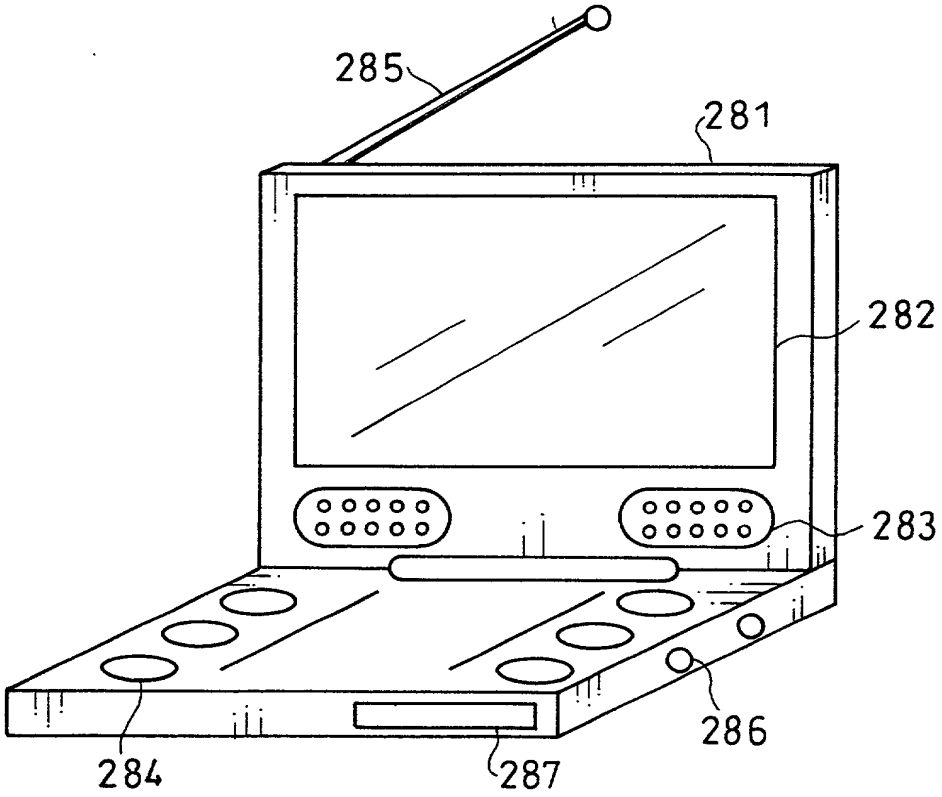

FIG. 91

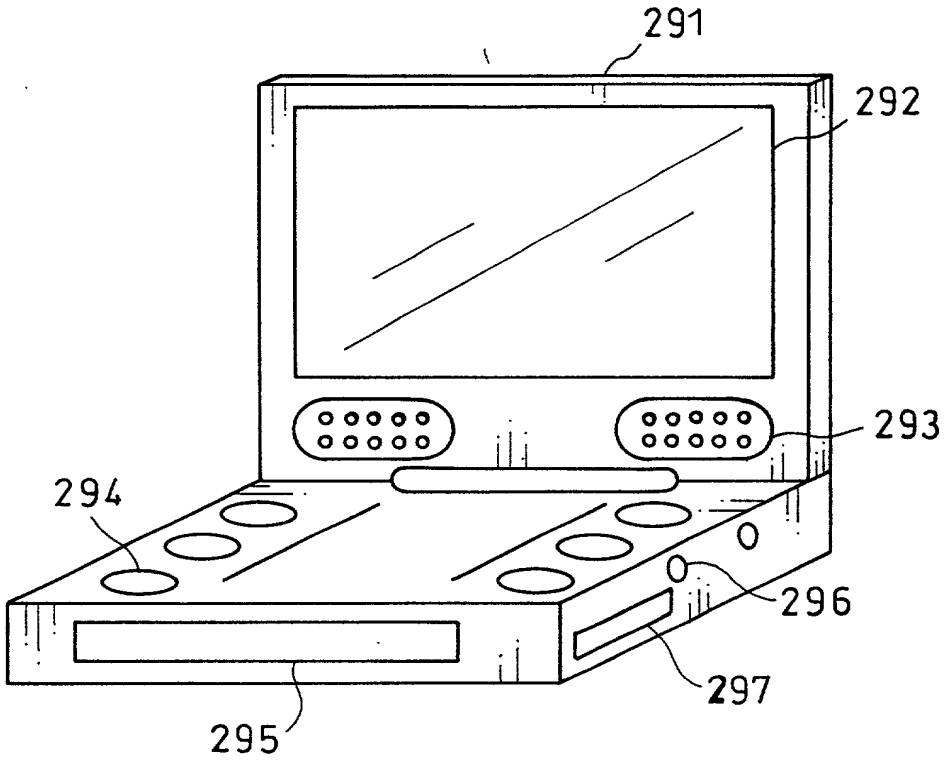

FIG. 92

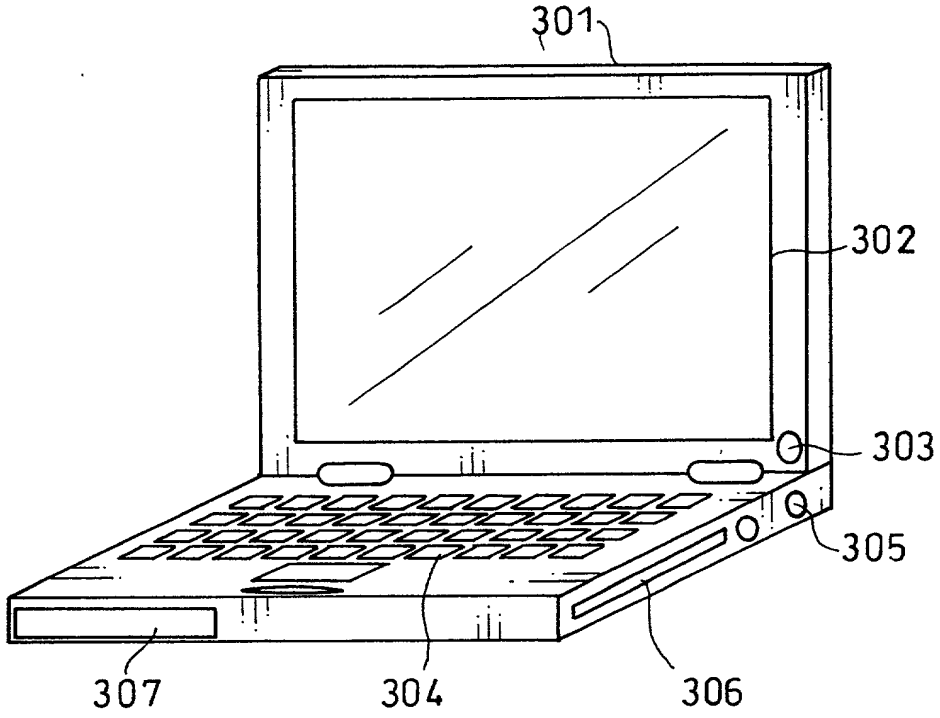

FIG. 93

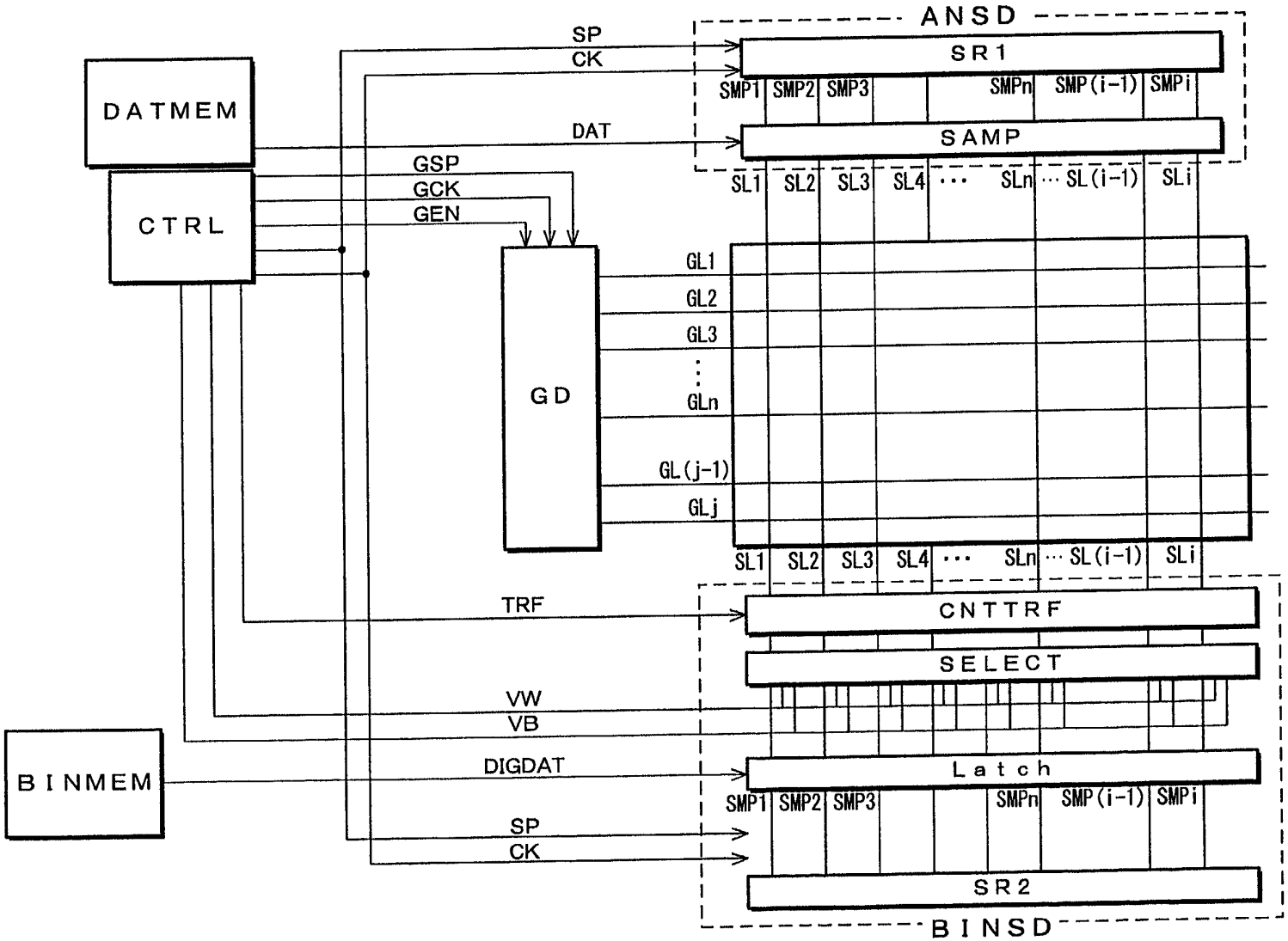
ANSD
SR1
SMP1
SMP2
SMP3
SMPn
SMP(i-1)
SMPi
SAMP
SL1
SL2
SL3
SL4
SLn
SL(i-1)
SLi
SP
CK
DAT
DATMEM
CTRL
GSP
GCK
GEN
GD
GL1
GL2
GL3
GLn
GL(j-1)
GLj
TRF
CNTTRF
SELECT
VW
VB
BINMEM
DIGDAT
Latch
SP
CK
SR2
BINSD

FIG. 94

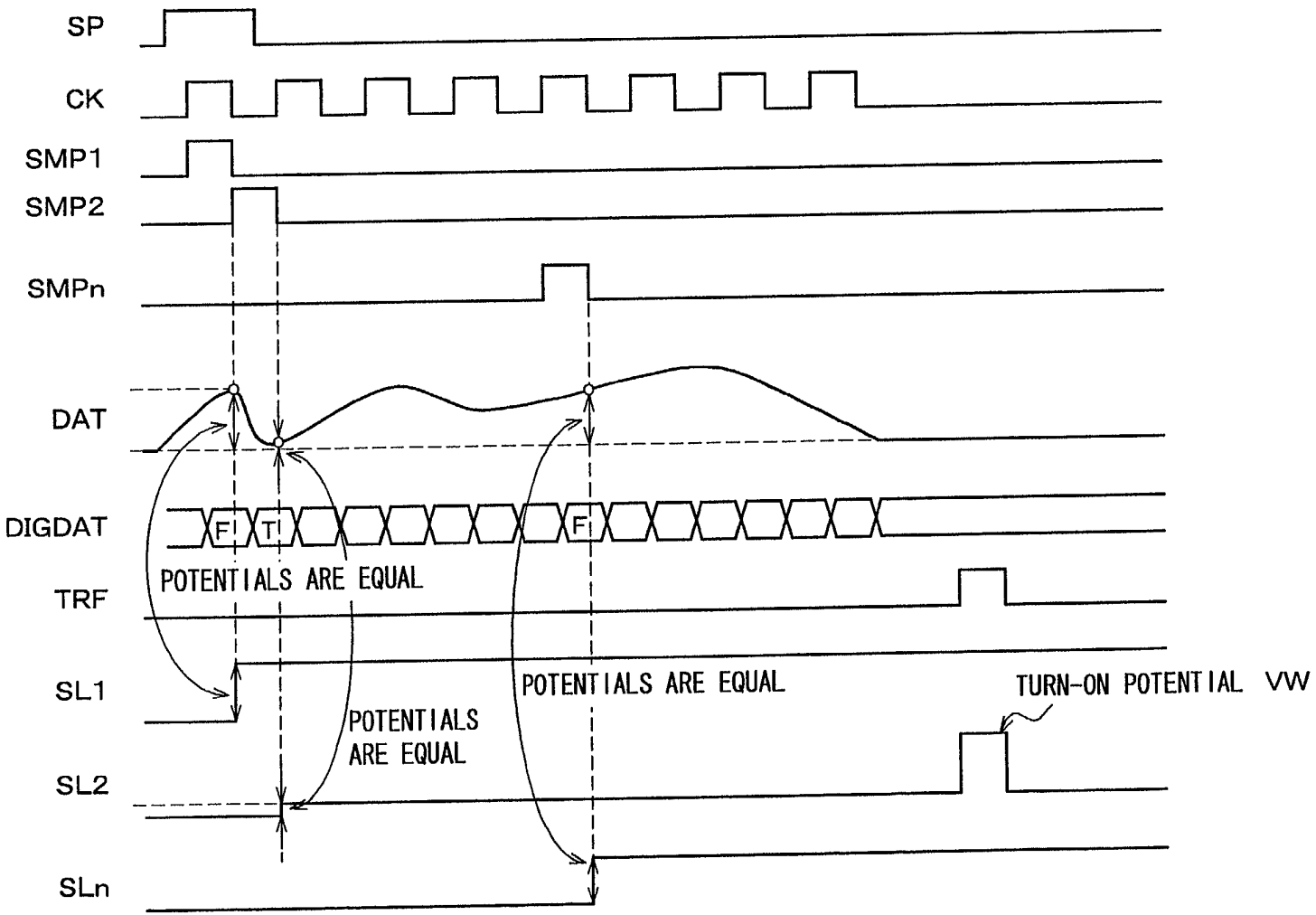
SP
CK
SMP1
SMP2
SMPn
DAT
DIGDAT
F
T
F
POTENTIALS ARE EQUAL
TRF
SL1
POTENTIALS ARE EQUAL
POTENTIALS ARE EQUAL
TURN-ON POTENTIAL VW
SL2
SLn

FIG. 95

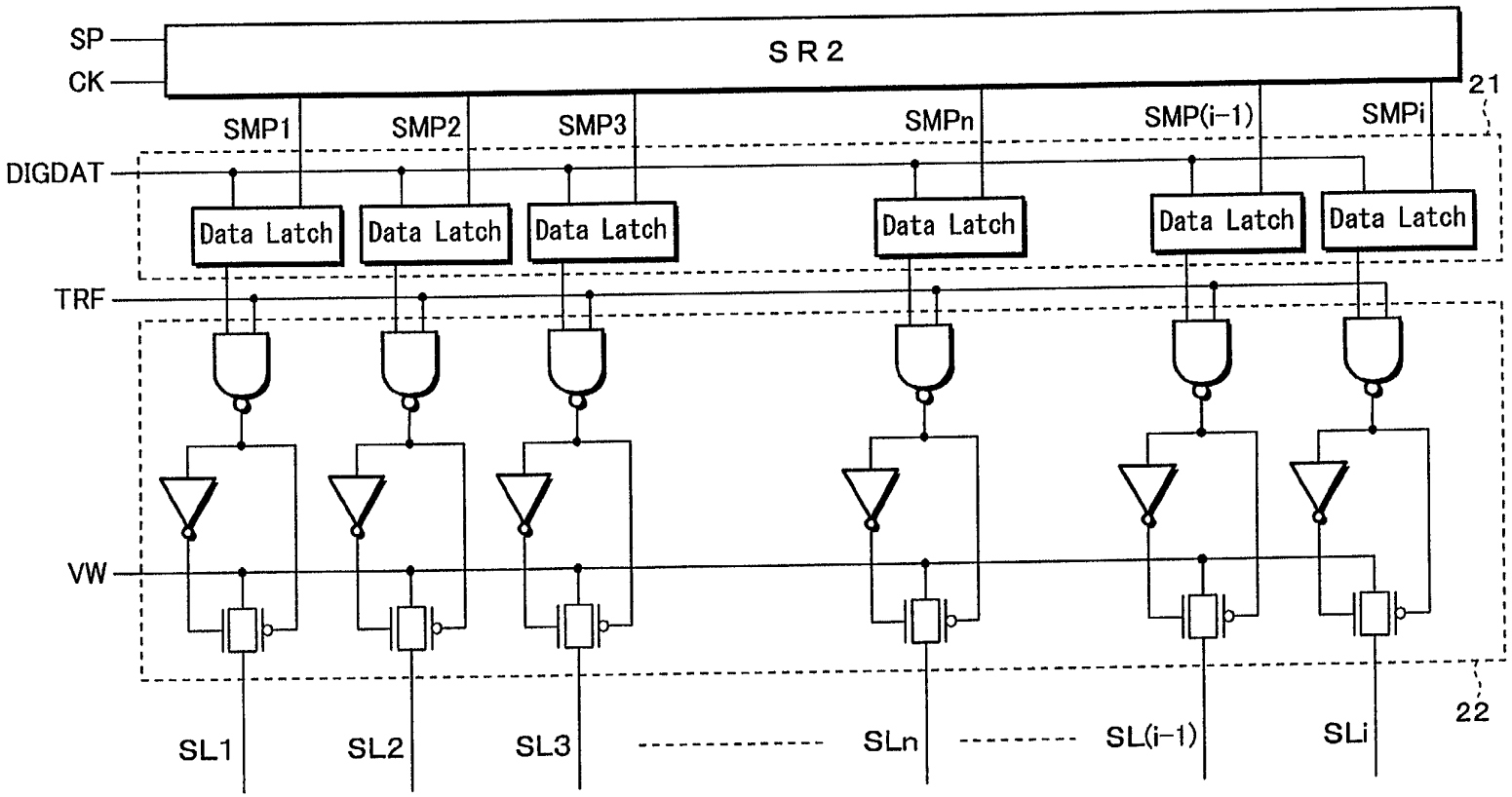
SP
CK
SR2
21
SMP1
SMP2
SMP3
SMPn
SMP(i-1)
SMPi
DIGDAT
Data Latch
Data Latch
Data Latch
Data Latch
Data Latch
Data Latch
TRF
VW
22
SL1
SL2
SL3
SLn
SL(i-1)
SLi

FIG. 96

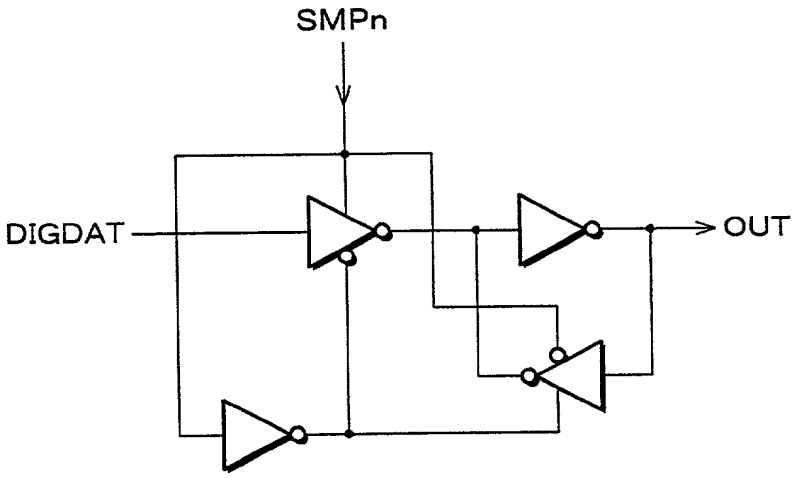

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FIG. 97

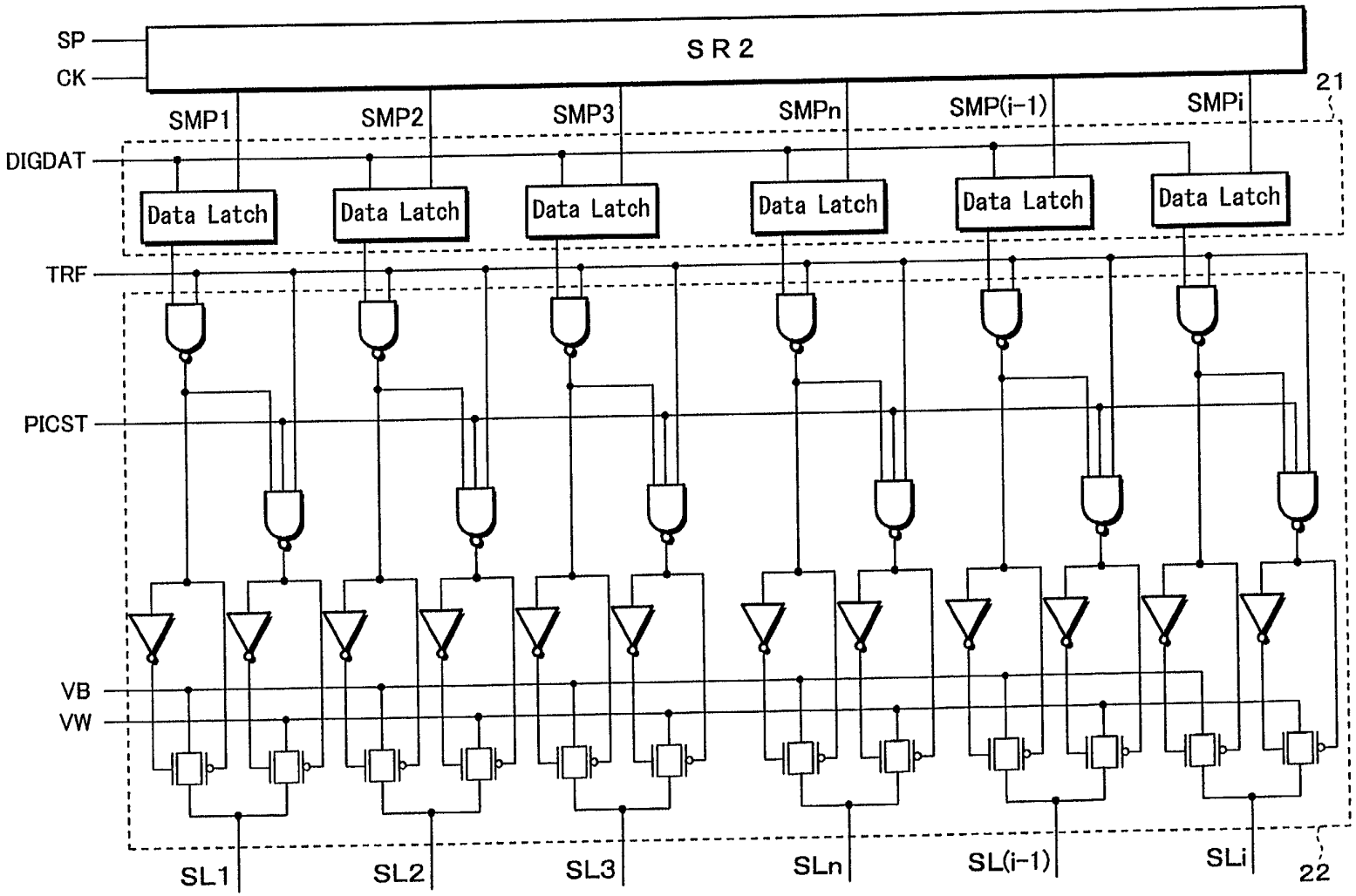
SP
CK
SR2
21
SMP1
SMP2
SMP3
SMPn
SMP(i-1)
SMPi
DIGDAT
Data Latch
Data Latch
Data Latch
Data Latch
Data Latch
Data Latch
TRF
PICST
VB
VW
SL1
SL2
SL3
SLn
SL(i-1)
SLi
22

FIG. 98

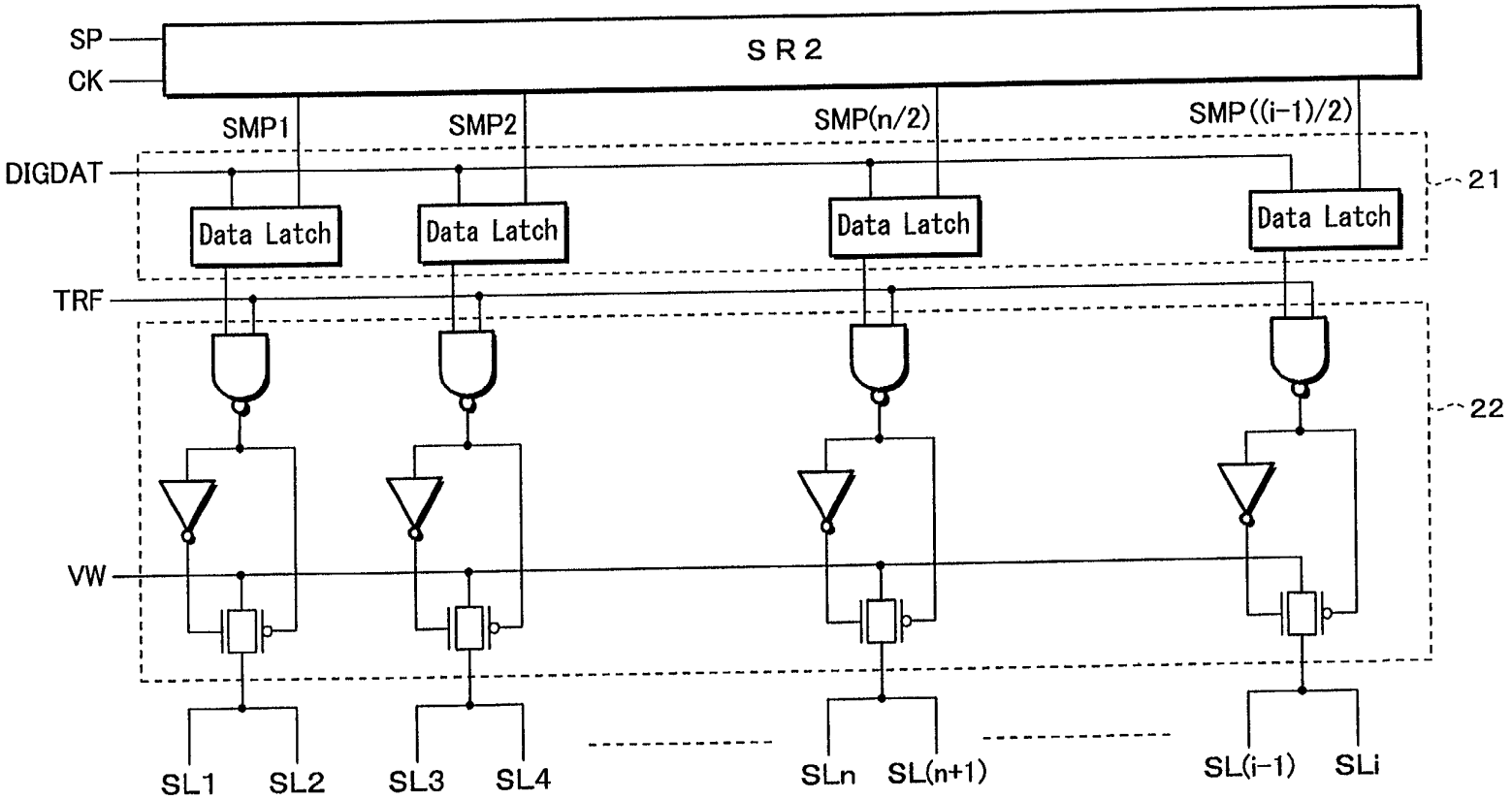
SP
CK
SR2
SMP1
SMP2
SMP(n/2)
SMP((i-1)/2)
DIGDAT
Data Latch
Data Latch
Data Latch
Data Latch
21
TRF
22
VW
SL1
SL2
SL3
SL4
SLn
SL(n+1)
SL(i-1)
SLi

FIG. 99

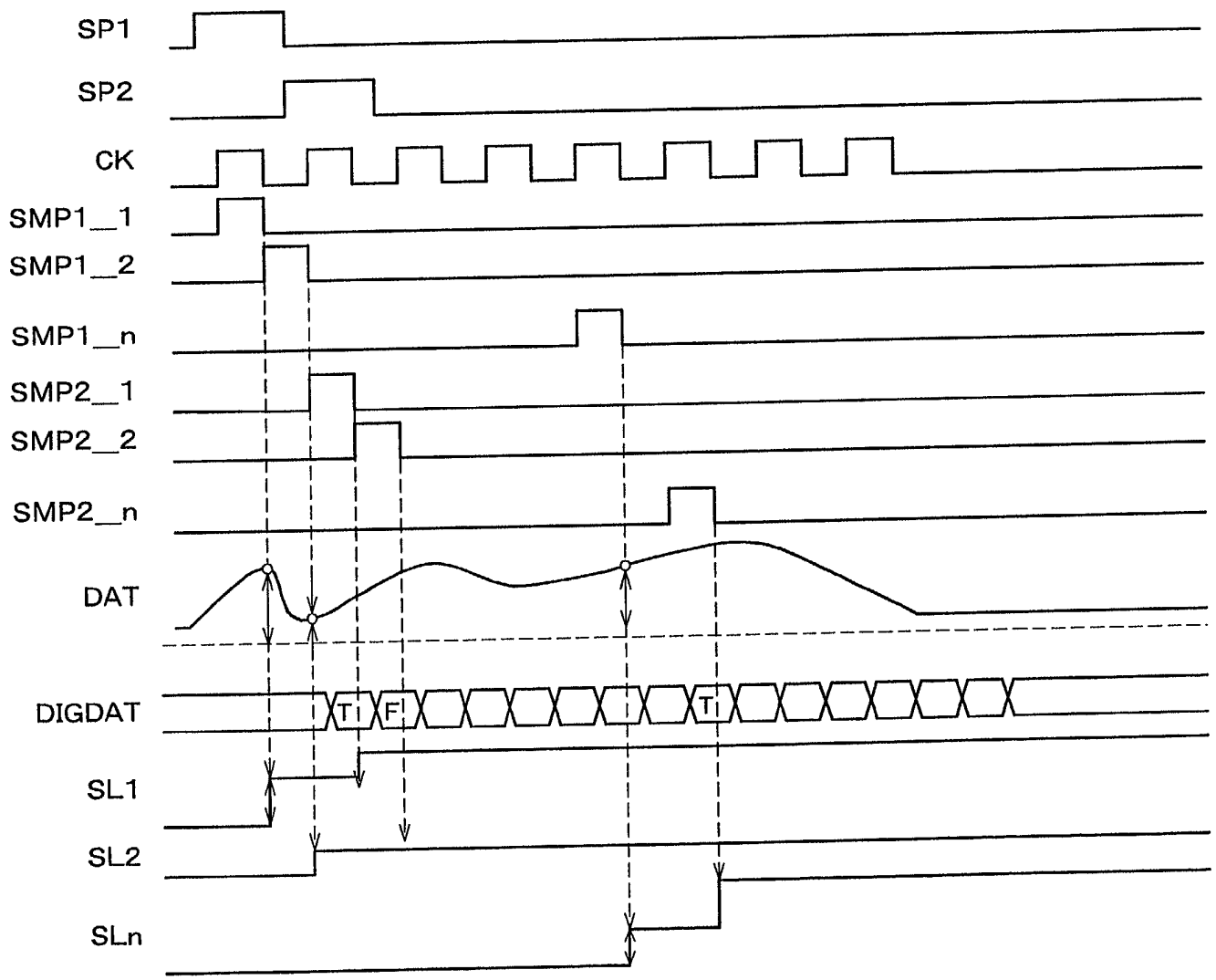
SP1
SP2
CK
SMP1__1
SMP1__2
SMP1__n
SMP2__1
SMP2__2
SMP2__n
DAT
DIGDAT
T
F
T
SL1
SL2
SLn

FIG. 100

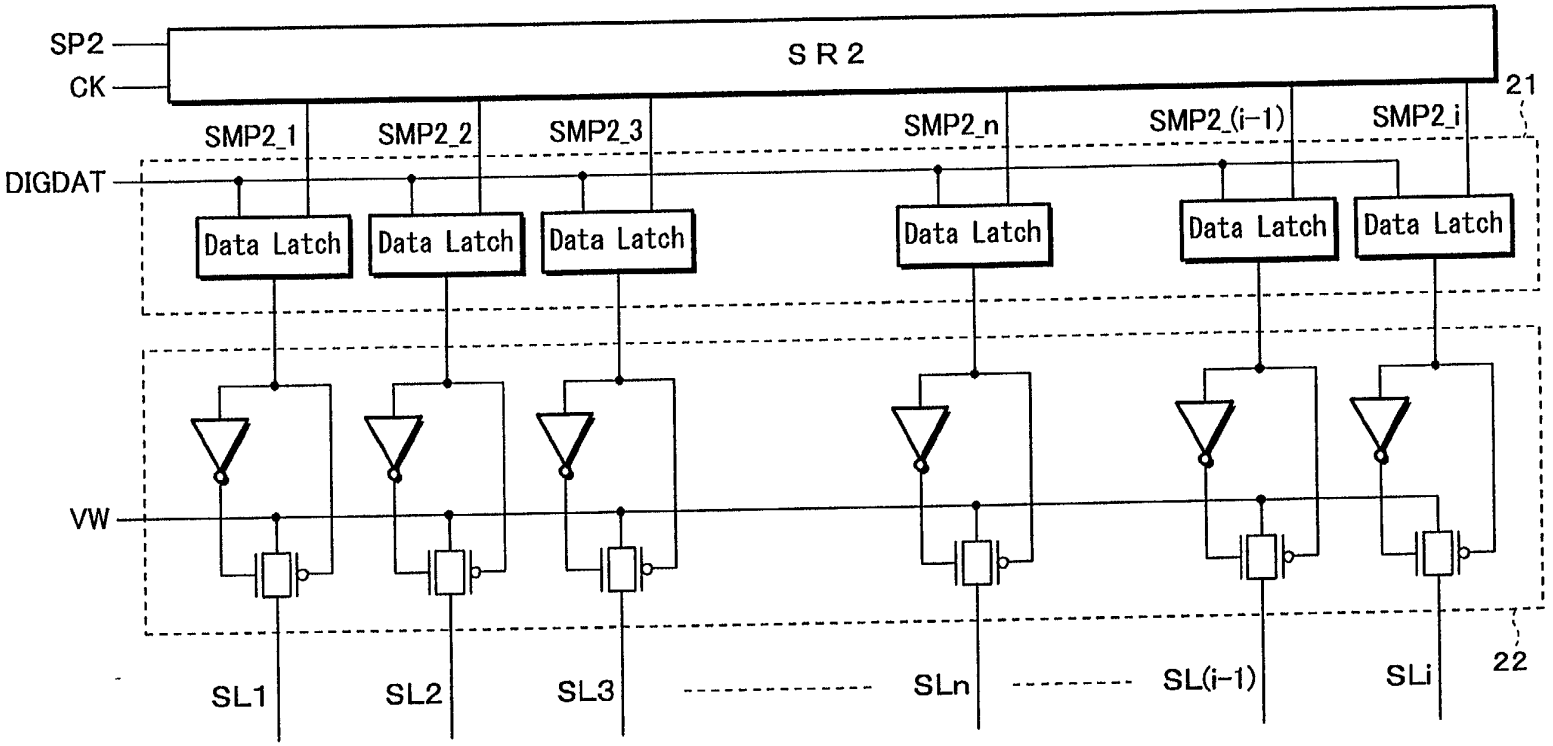
SP2
CK
SR2
21
SMP2_1
SMP2_2
SMP2_3
SMP2_n
SMP2_(i-1)
SMP2_i
DIGDAT
Data Latch
Data Latch
Data Latch
Data Latch
Data Latch
Data Latch
VW
22
SL1
SL2
SL3
SLn
SL(i-1)
SLi

FIG. 101

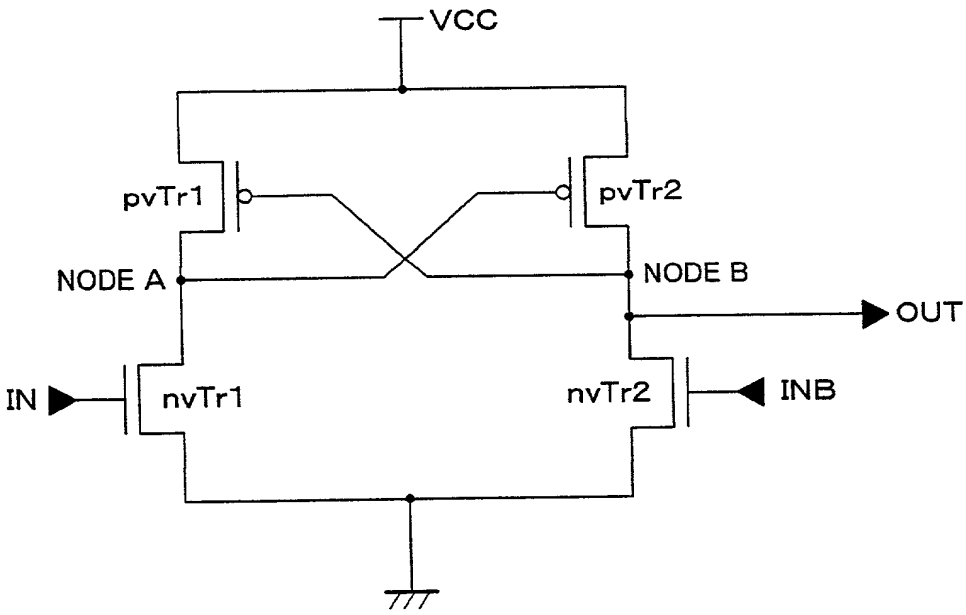

FIG. 102

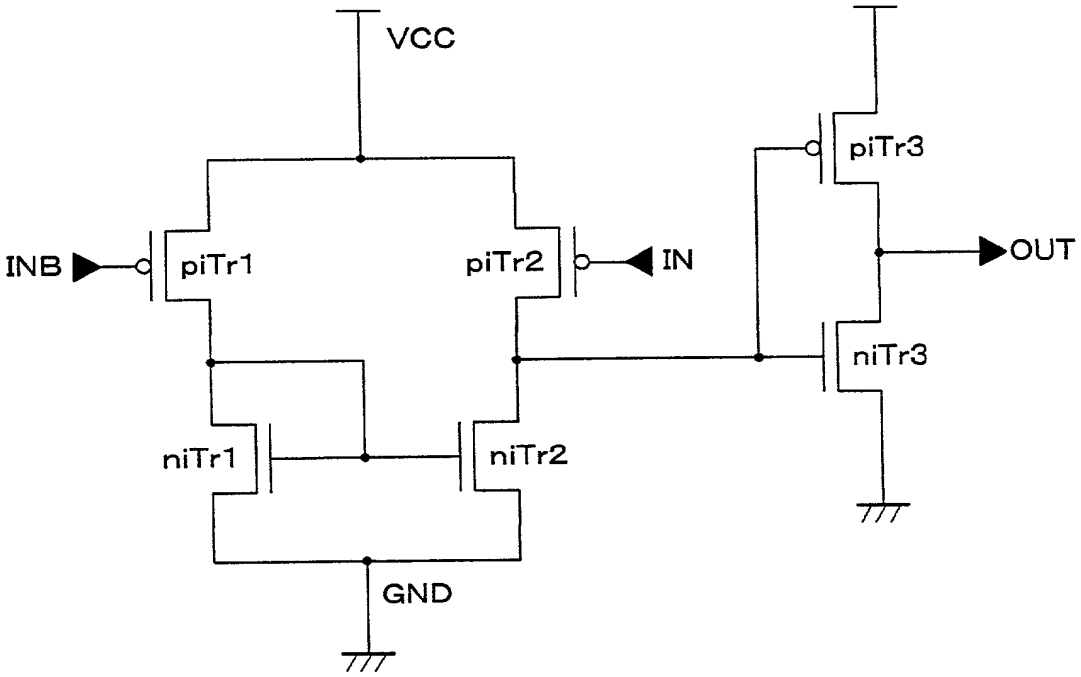

FIG. 103

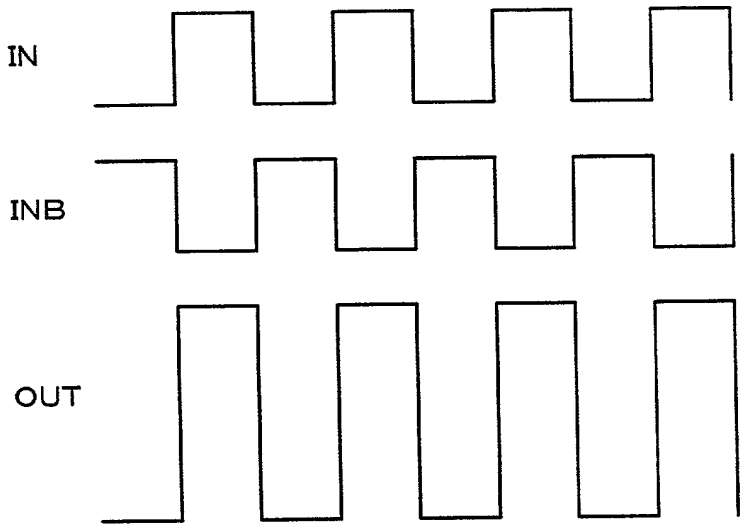

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FIG. 104

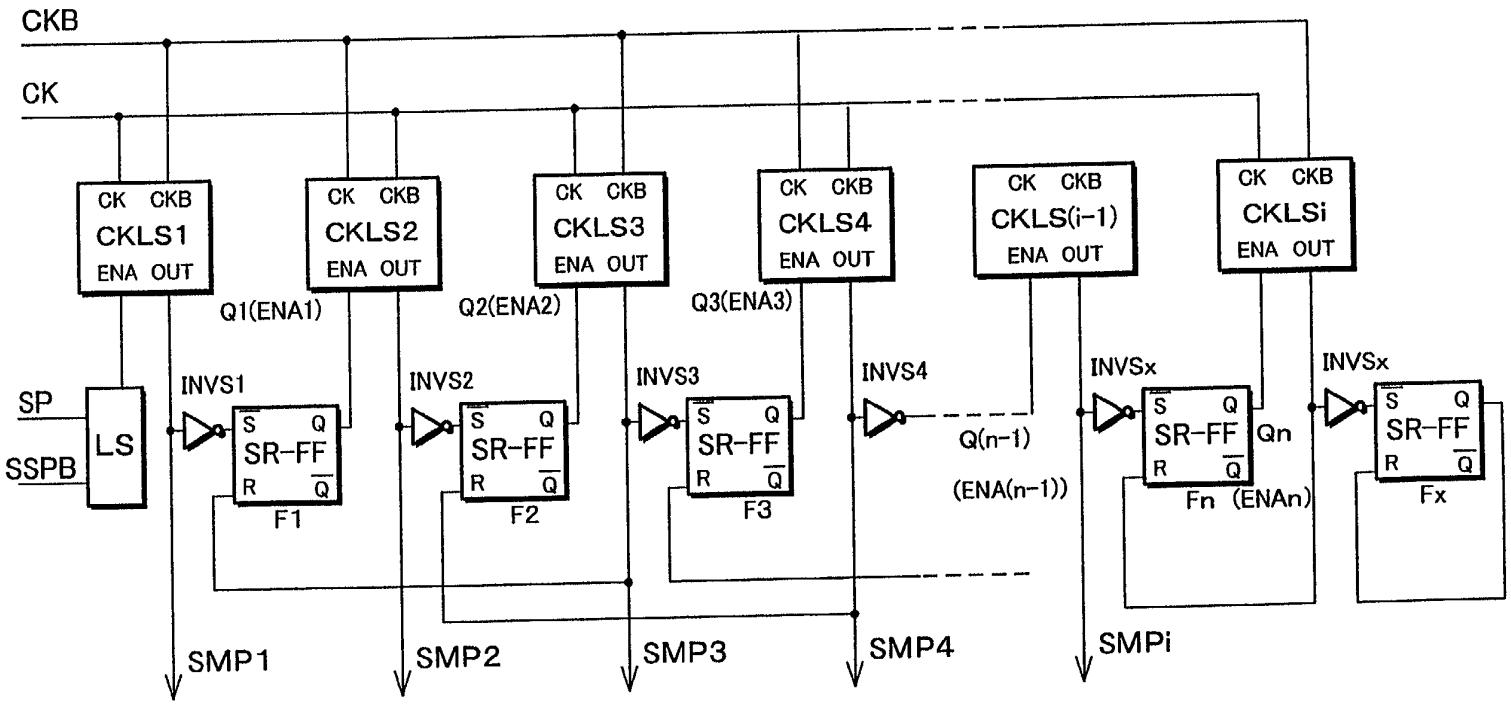
CKB
CK
CK CKB
CKLS1
ENA OUT
CK CKB
CKLS2
ENA OUT
CK CKB
CKLS3
ENA OUT
CK CKB
CKLS4
ENA OUT
CK CKB
CKLS(i-1)
ENA OUT
CK CKB
CKLSi
ENA OUT
Q1(ENA1)
Q2(ENA2)
Q3(ENA3)
SP
SSPB
LS
INVS1
INVS2
INVS3
INVS4
INVSx
INVSx
S Q
SR-FF
R Q
F1
F2
F3
Q(n-1)
(ENA(n-1))
Qn
Fn (ENAn)
Fx
SMP1
SMP2
SMP3
SMP4
SMPi

FIG. 105

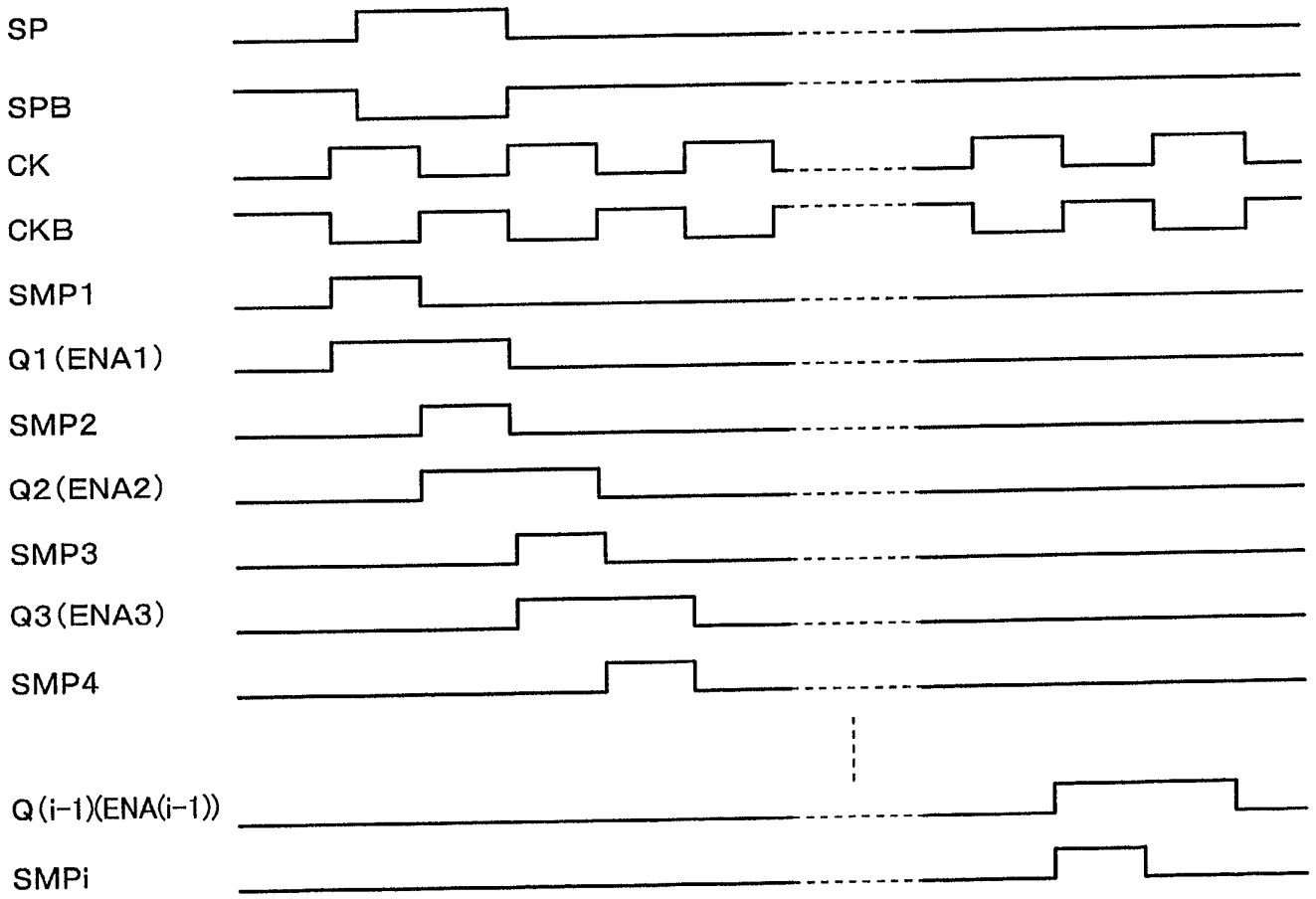
SP
SPB
CK
CKB
SMP1
Q1(ENA1)
SMP2
Q2(ENA2)
SMP3
Q3(ENA3)
SMP4
Q(i-1)(ENA(i-1))
SMPi

FIG. 106 (a)

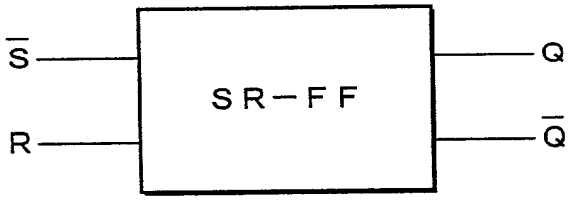

FIG. 106 (b)

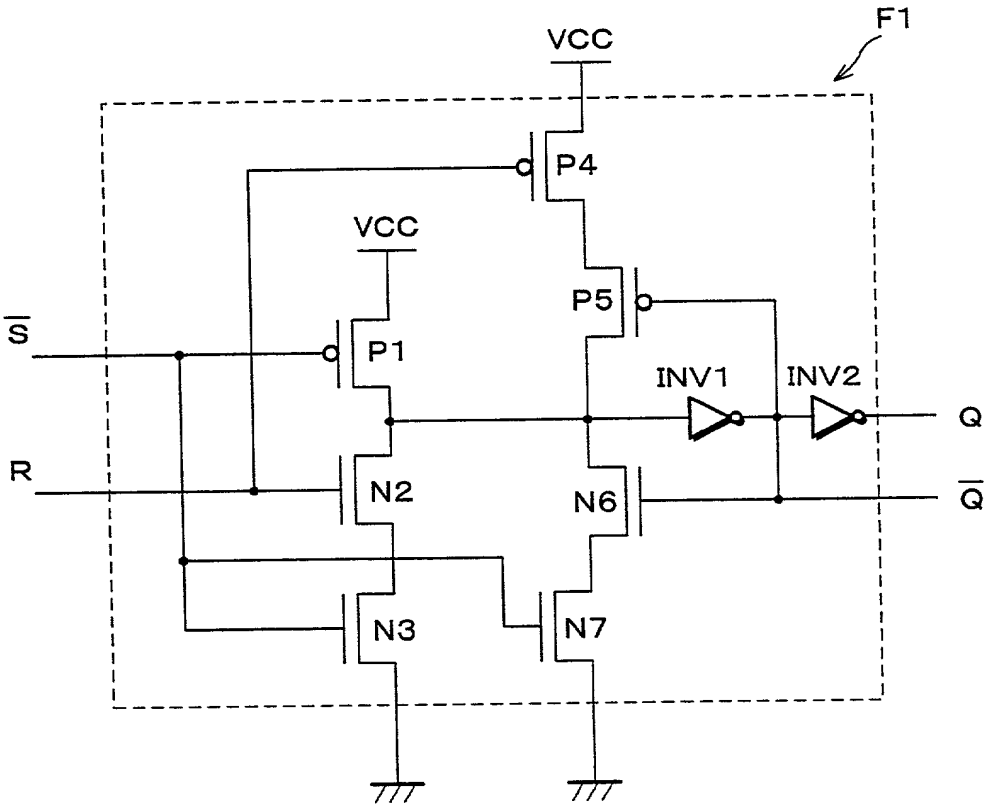

FIG. 107

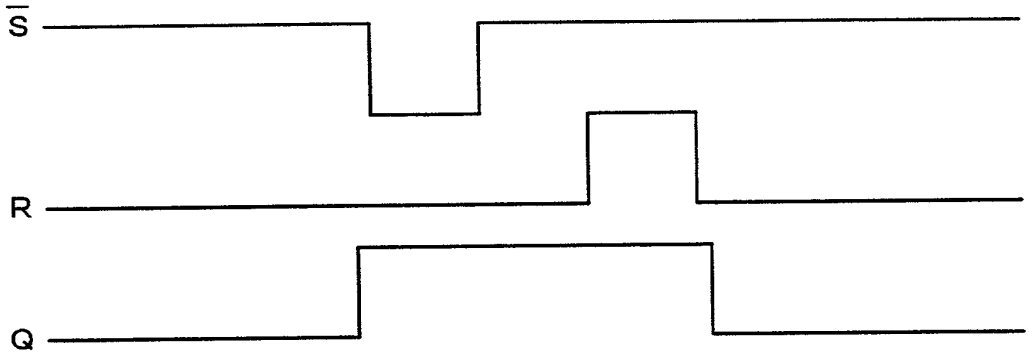

FIG. 108

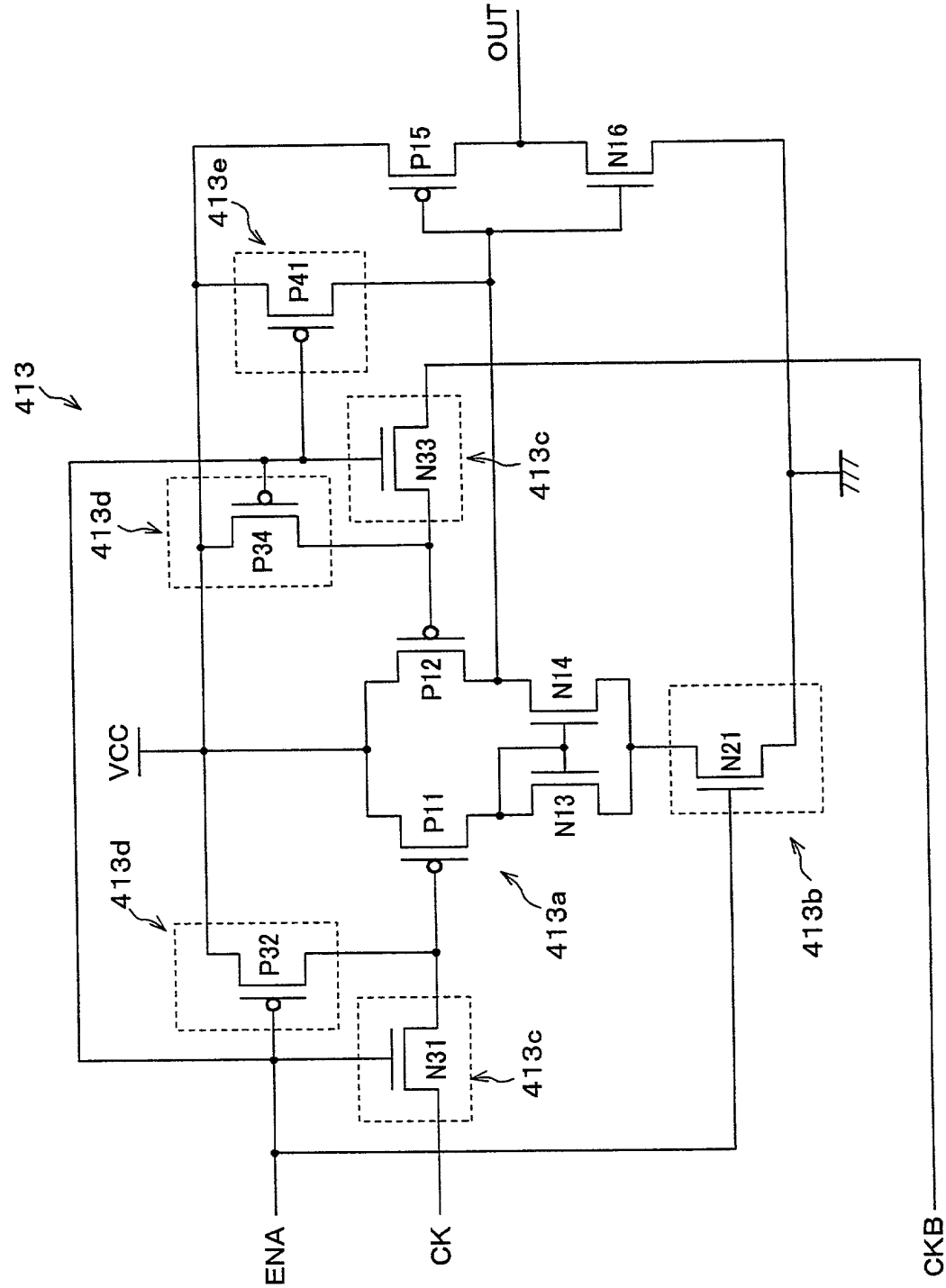
413
413e
P41
P15
N16
OUT
413d
P34
N33
413c
VCC
P12
N14
P11
N13
N21
413d
P32
413a
413b
N31
413c
ENA
CK
CKB

FIG. 109

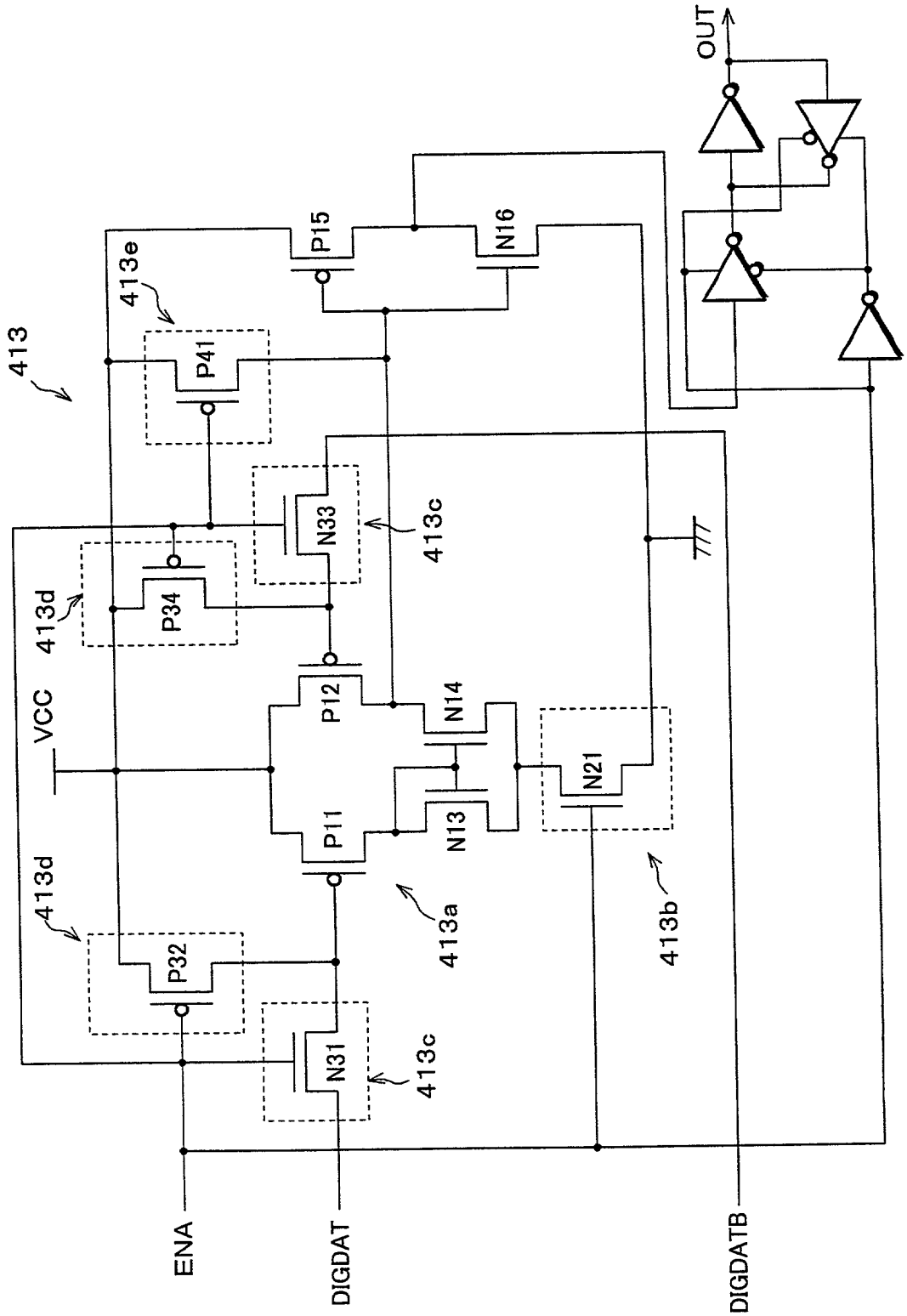
413
413e
P41
P15
N16
OUT
413d
P34
N33
413c
VCC
P12
N14
413d
P32
P11
N13
N21
413a
413b
413c
N31
ENA
DIGDAT
DIGDATB

FIG. 110

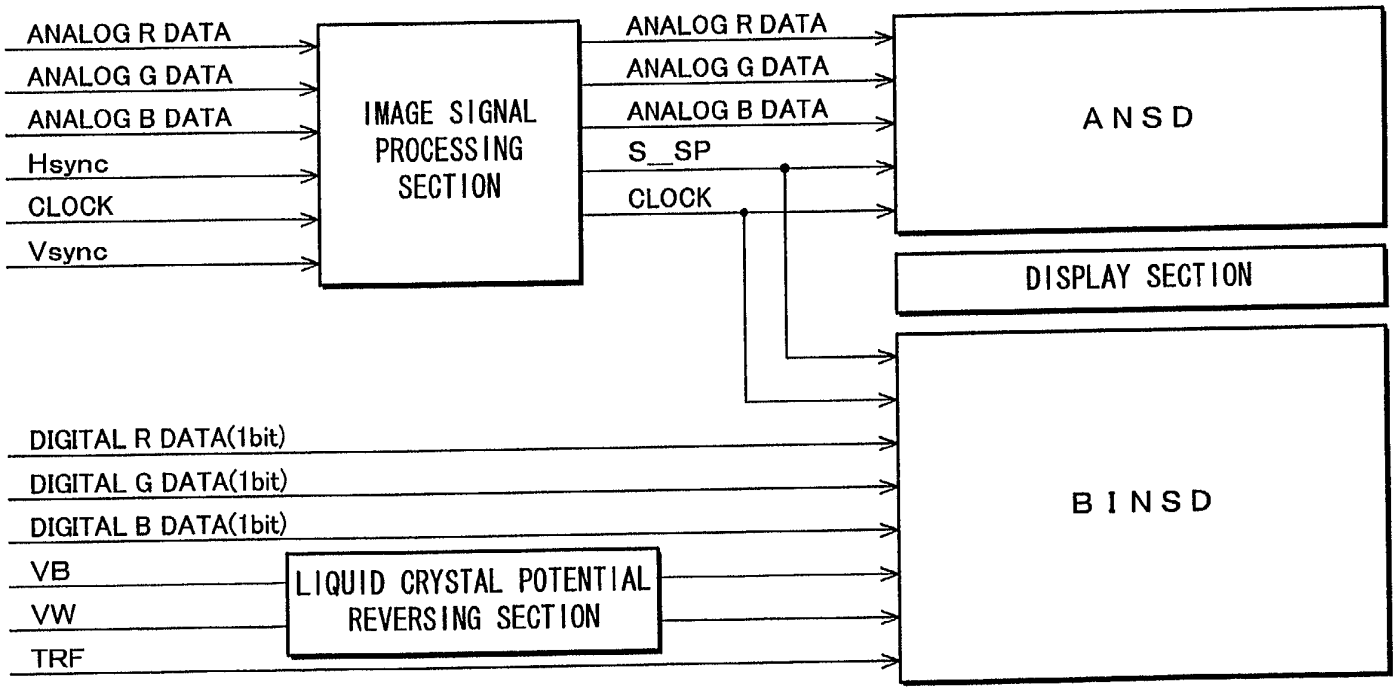
ANALOG R DATA
ANALOG G DATA
ANALOG B DATA
Hsync
CLOCK
Vsync
IMAGE SIGNAL PROCESSING SECTION
ANALOG R DATA
ANALOG G DATA
ANALOG B DATA
S_SP
CLOCK
ANSD
DISPLAY SECTION
DIGITAL R DATA(1bit)
DIGITAL G DATA(1bit)
DIGITAL B DATA(1bit)
VB
VW
TRF
LIQUID CRYSTAL POTENTIAL REVERSING SECTION
BINSD

FIG. 111

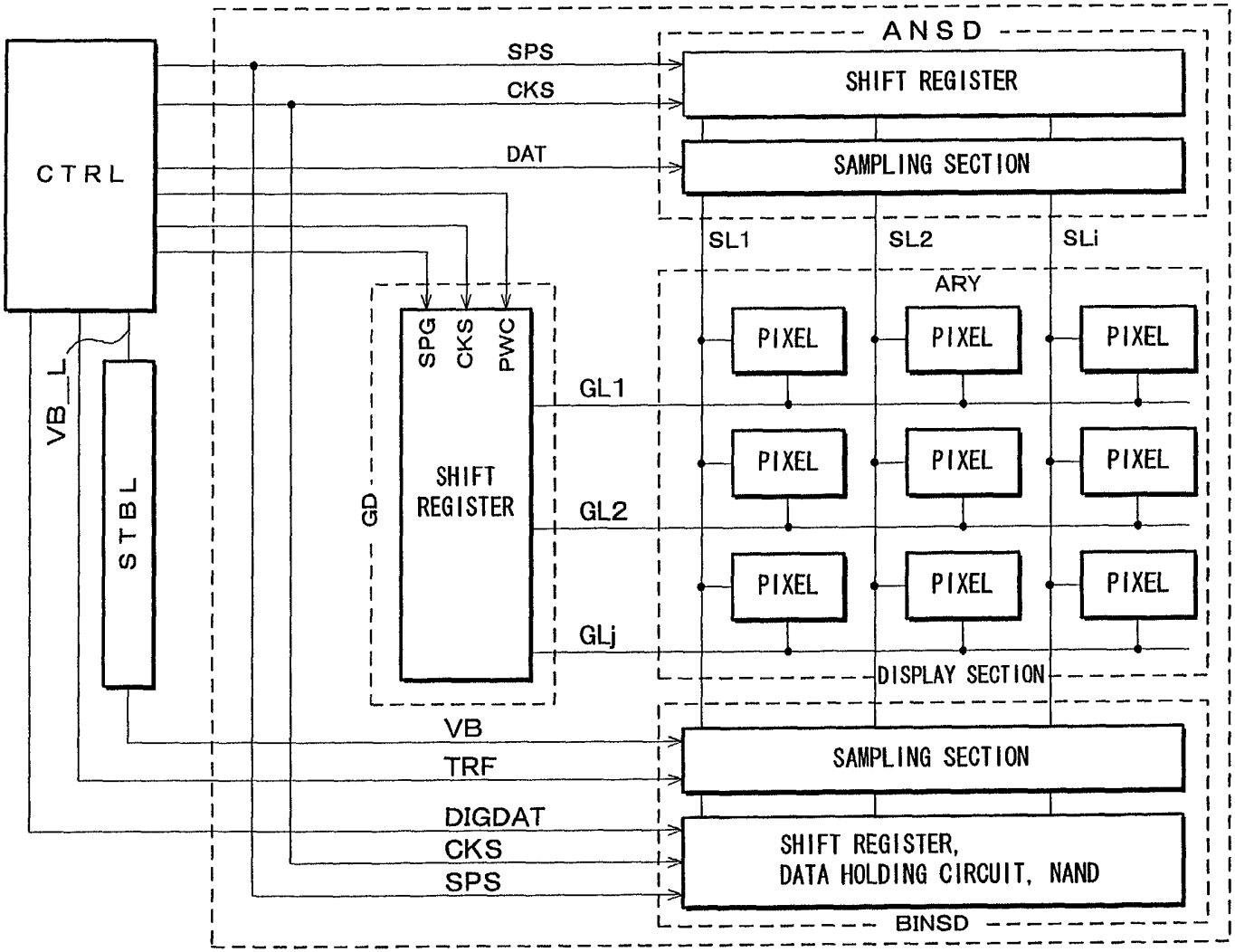
ANSD
SPS
CKS
DAT
CTRL
SHIFT REGISTER
SAMPLING SECTION
SL1
SL2
SLi
ARY
PIXEL
VB_L
STBL
SPG
CKS
PWC
GD
SHIFT REGISTER
GL1
GL2
GLj
DISPLAY SECTION
VB
TRF
DIGDAT
CKS
SPS
SAMPLING SECTION
SHIFT REGISTER,
DATA HOLDING CIRCUIT, NAND
BINSD

FIG. 112

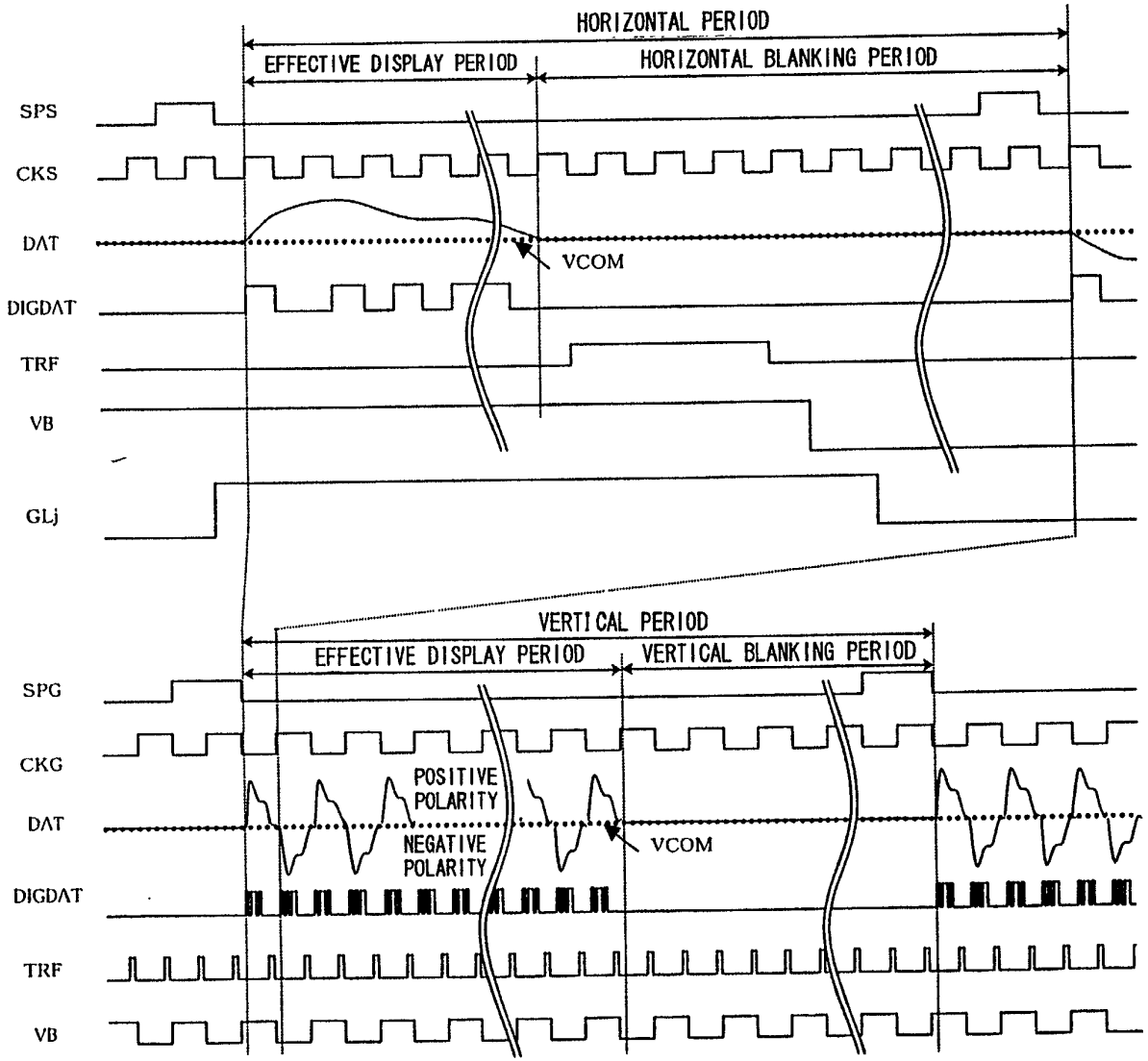
HORIZONTAL PERIOD
EFFECTIVE DISPLAY PERIOD
HORIZONTAL BLANKING PERIOD
SPS
CKS
DAT
VCOM
DIGDAT
TRF
VB
GLj
VERTICAL PERIOD
EFFECTIVE DISPLAY PERIOD
VERTICAL BLANKING PERIOD
SPG
CKG
POSITIVE POLARITY
DAT
NEGATIVE POLARITY
VCOM
DIGDAT
TRF
VB

FIG. 113

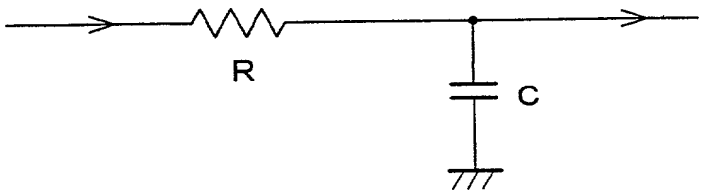

Fig. 113 of 115

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FIG. 114

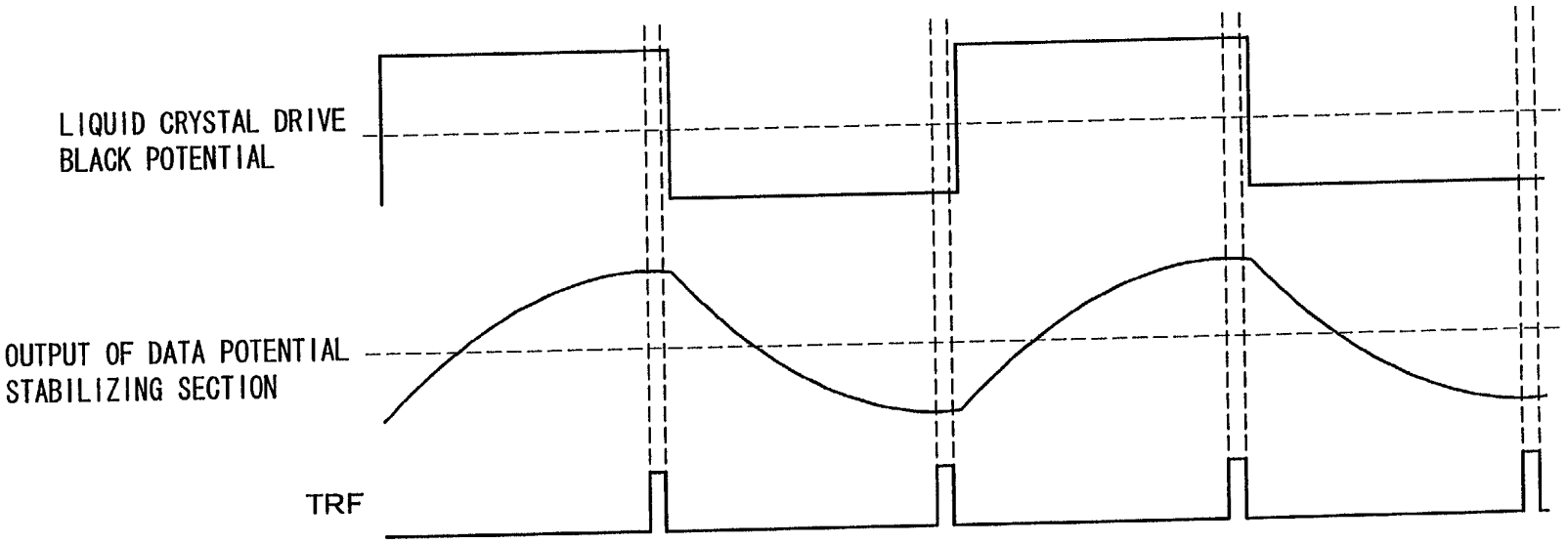

FIG. 115

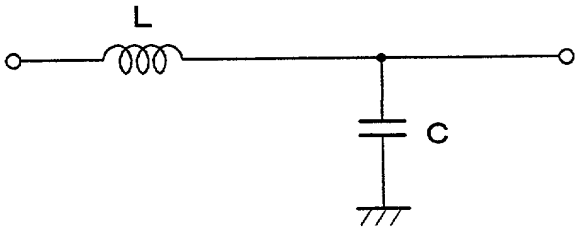

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FIG. 116

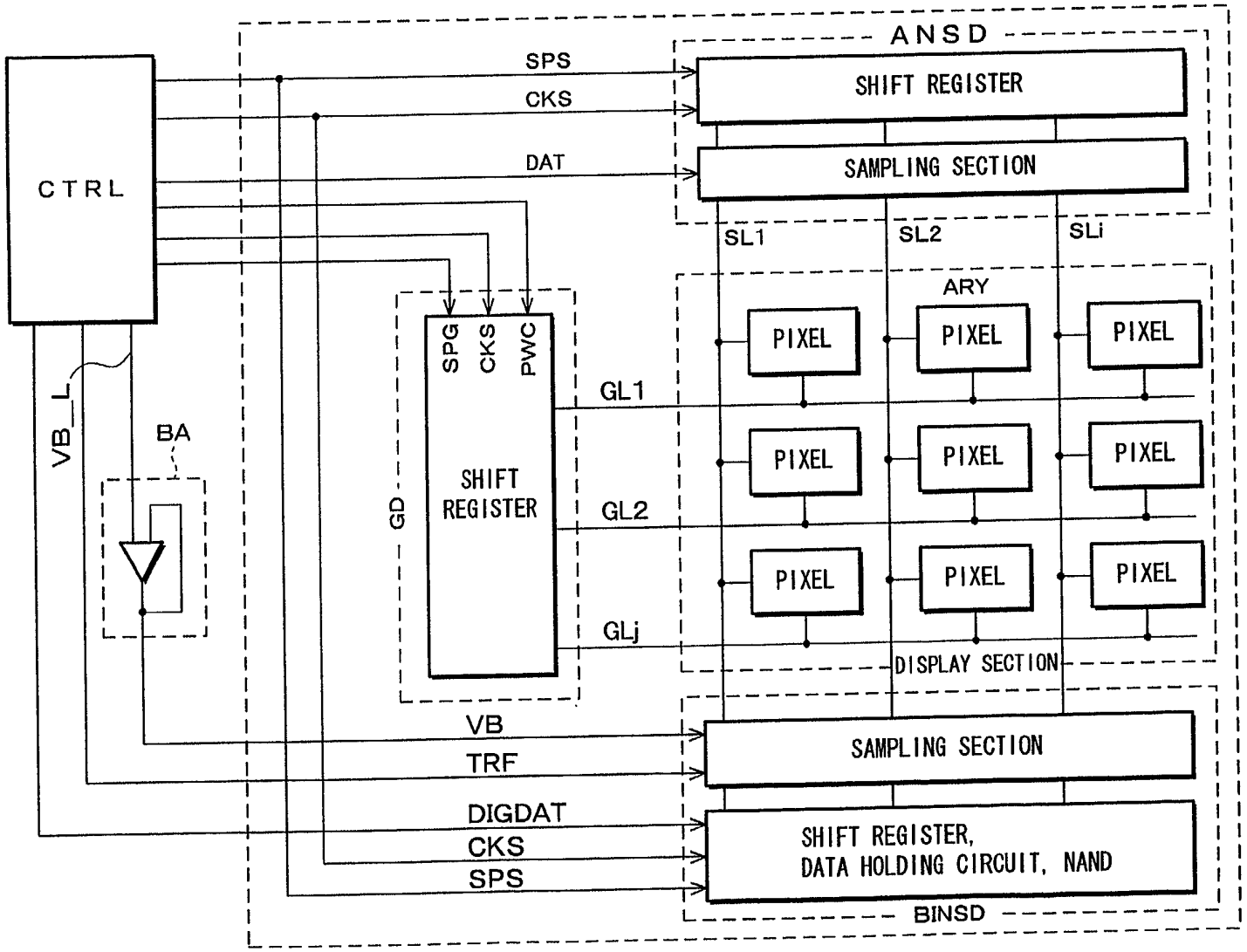
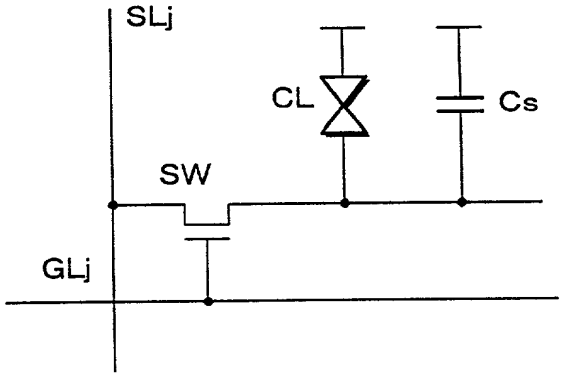
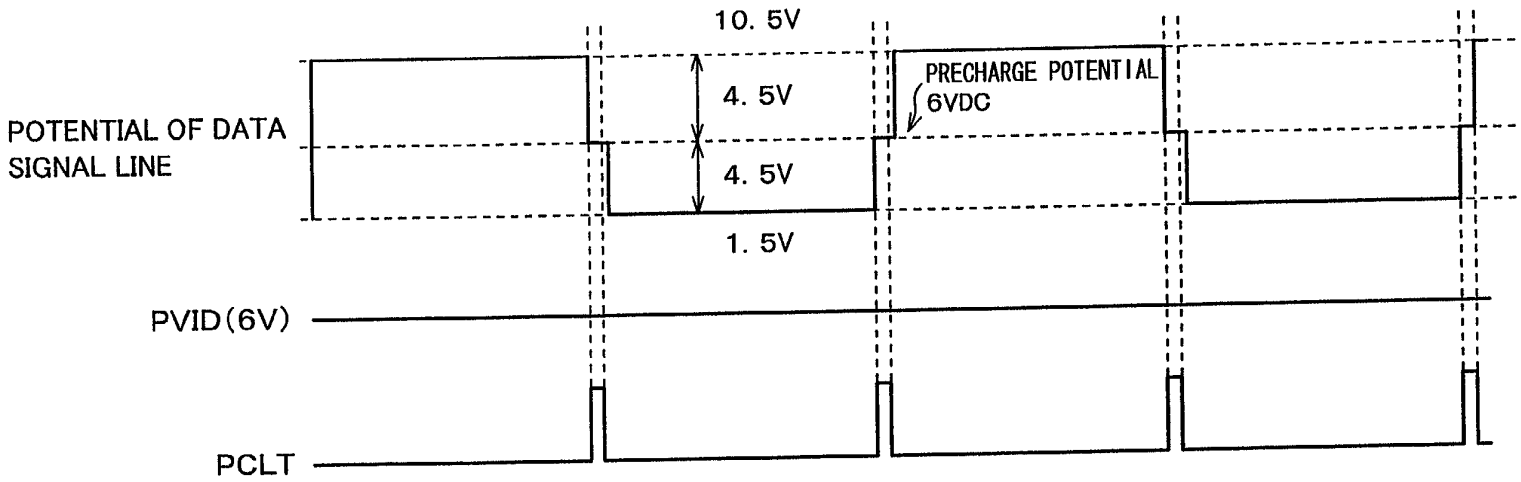

ANSD
SPS
CKS
DAT
CTRL
SHIFT REGISTER
SAMPLING SECTION
SL1
SL2
SLi
ARY
SPG
CKS
PWC
PIXEL
GL1
GL2
GLj
VB_L
BA
SHIFT REGISTER
GD
DISPLAY SECTION
VB
TRF
DIGDAT
CKS
SPS
SAMPLING SECTION
SHIFT REGISTER,
DATA HOLDING CIRCUIT, NAND
BINSD

FIG. 117



JP2005050356A

FIG. 118



FOCUS SOFTWARE

FIG. 119

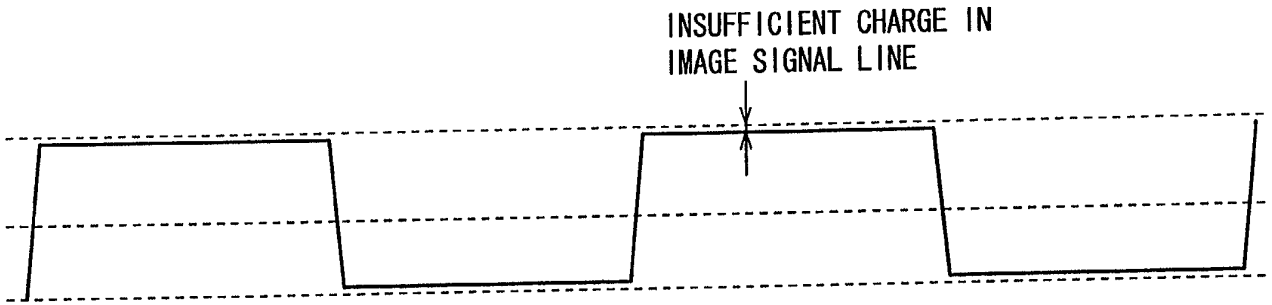
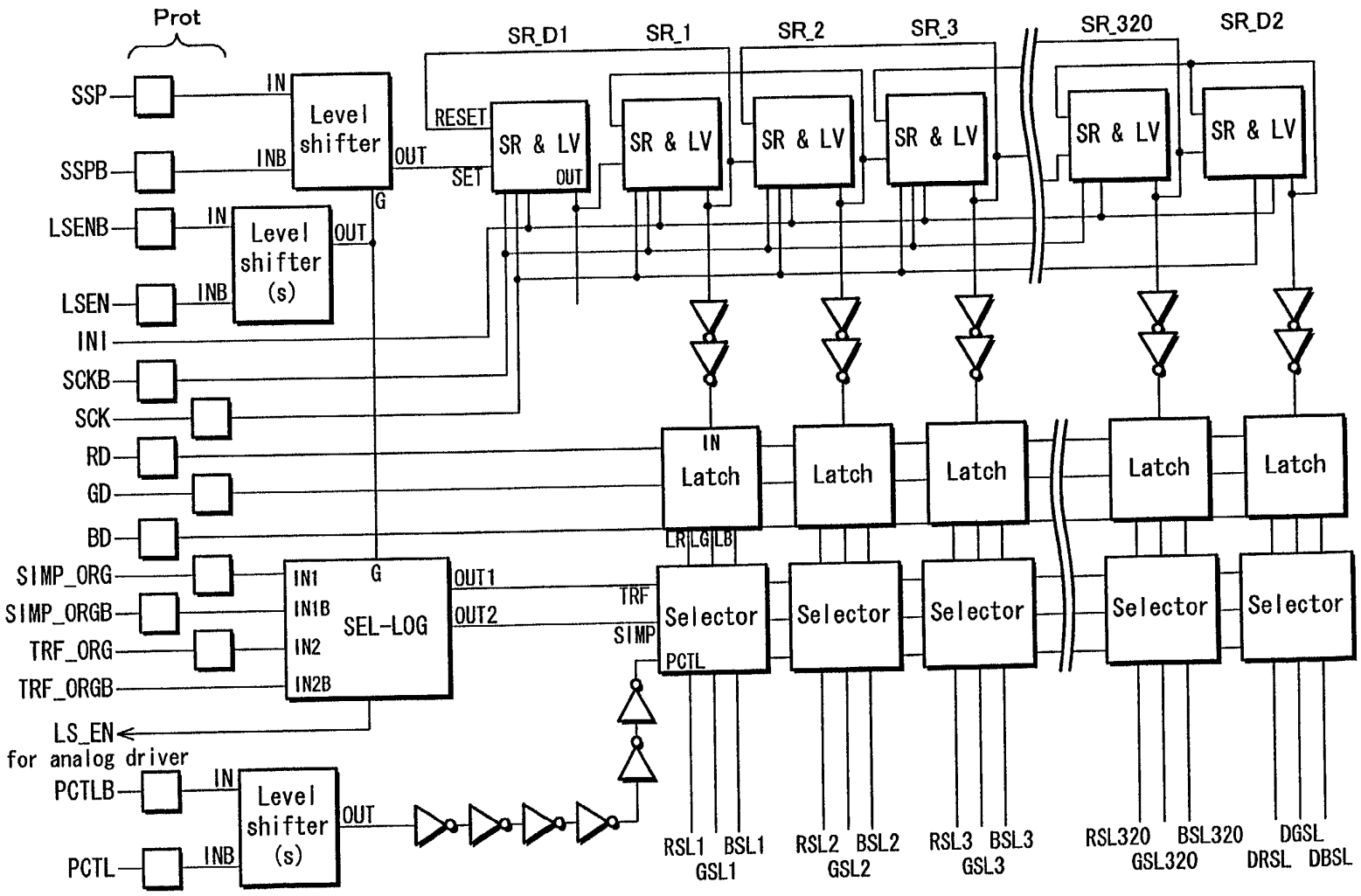


FIG. 120


Prot
SSP
SSPB
LSENB
LSEN
INI
SCKB
SCK
RD
GD
BD
SIMP_ORG
SIMP_ORGB
TRF_ORG
TRF_ORGB
LS_EN
for analog driver
PCTLB
PCTL
IN
INB
Level shifter
Level shifter (s)
OUT
G
SR_D1
SR_1
SR_2
SR_3
SR_320
SR_D2
RESET
SET
SR & LV
OUT
IN Latch
Latch
LR
LG
LB
IN1
IN1B
IN2
IN2B
SEL-LOG
OUT1
OUT2
TRF
SIMP
PCTL
Selector
RSL1
BSL1
GSL1
RSL2
BSL2
GSL2
RSL3
BSL3
GSL3
RSL320
BSL320
GSL320
DGSL
DRSL
DBSL

TOSHIBA 5887586D

FIG. 121

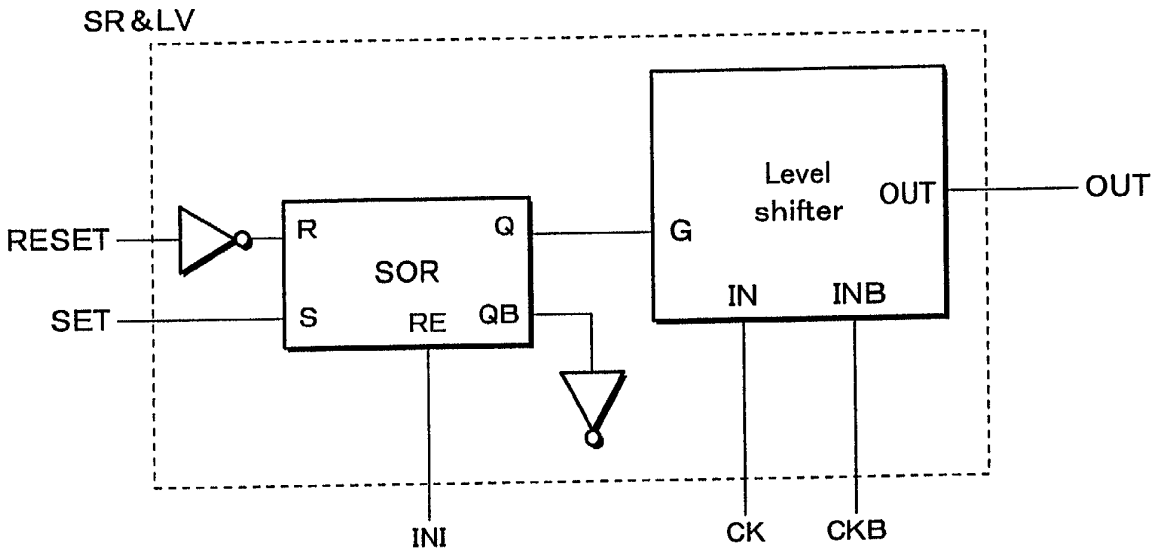


FIG. 122

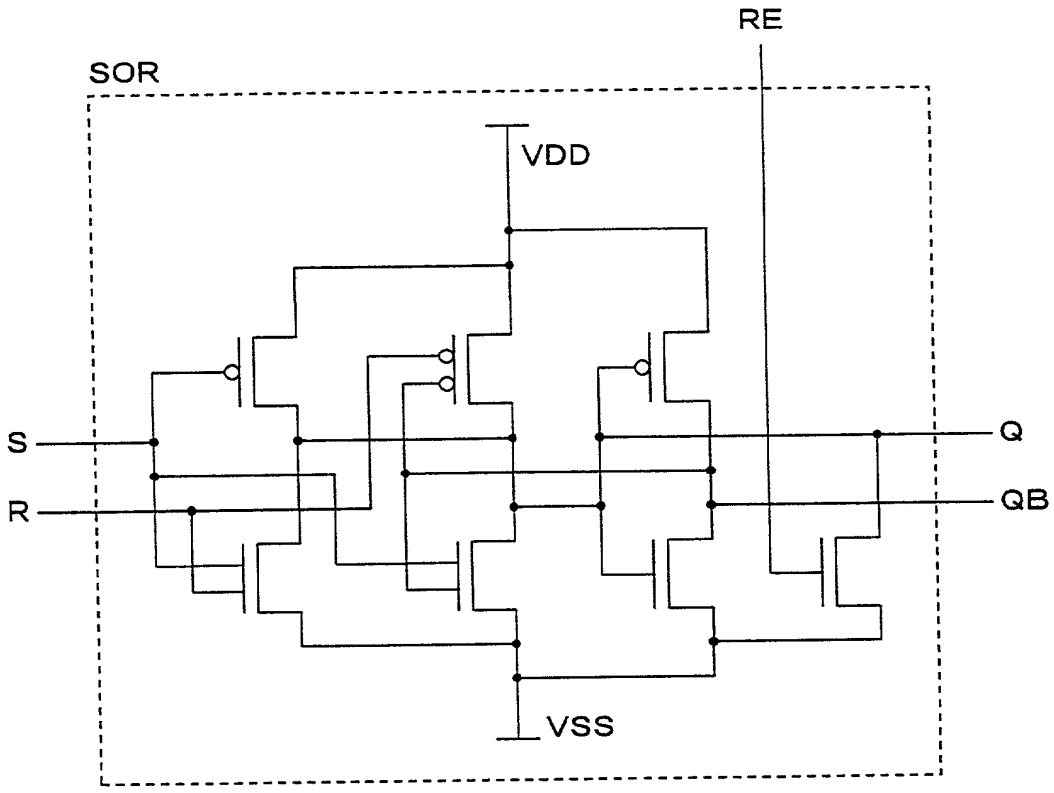


FIG. 123

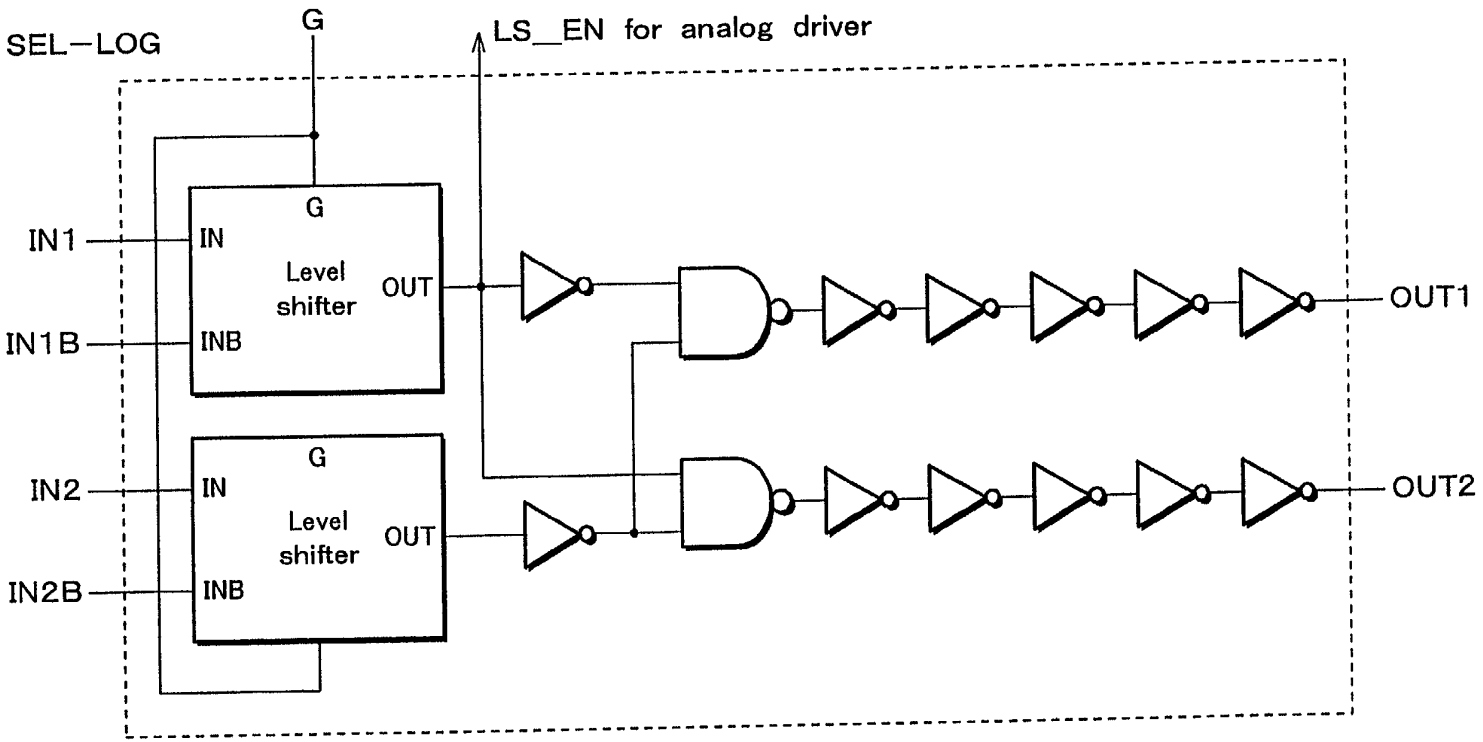

SEL—LOG
G
LS_EN for analog driver
G
IN1
IN
Level shifter
OUT
IN1B
INB
OUT1
G
IN2
IN
Level shifter
OUT
IN2B
INB
OUT2

FIG. 124

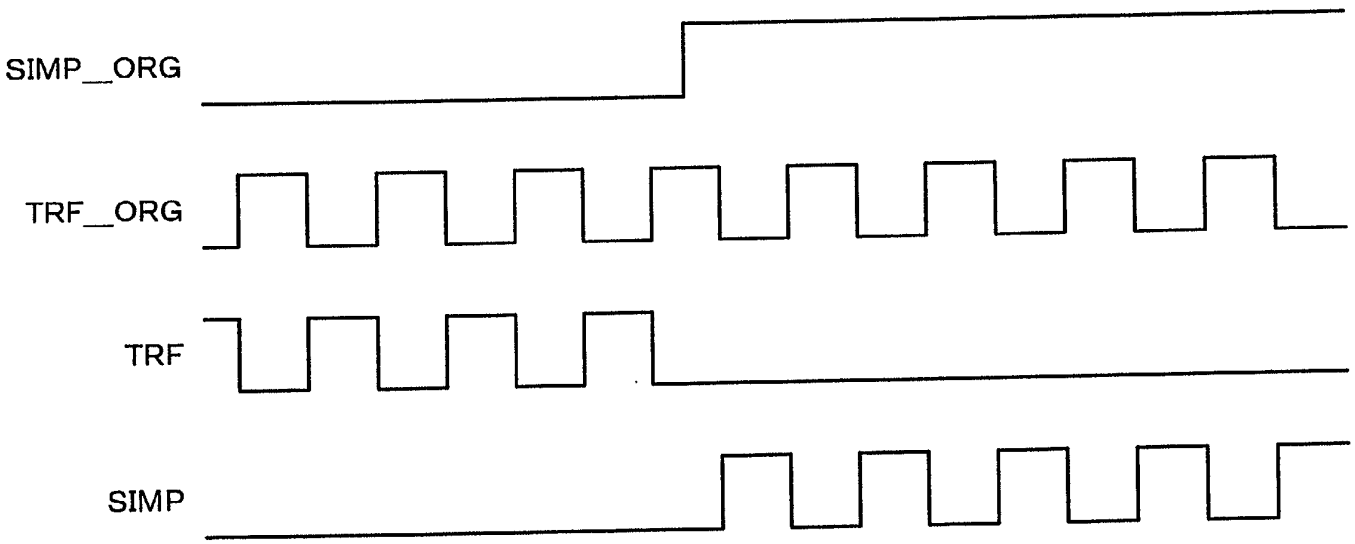
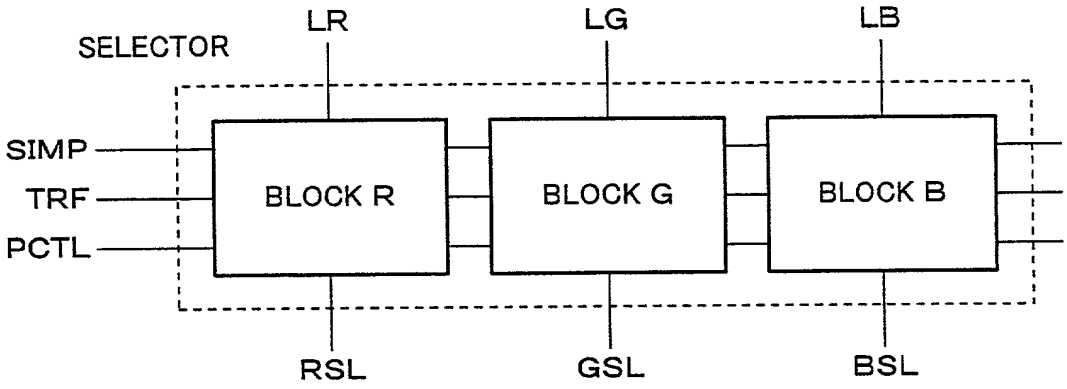


FIG. 125



EP 3 637 754 A1

FIG. 126

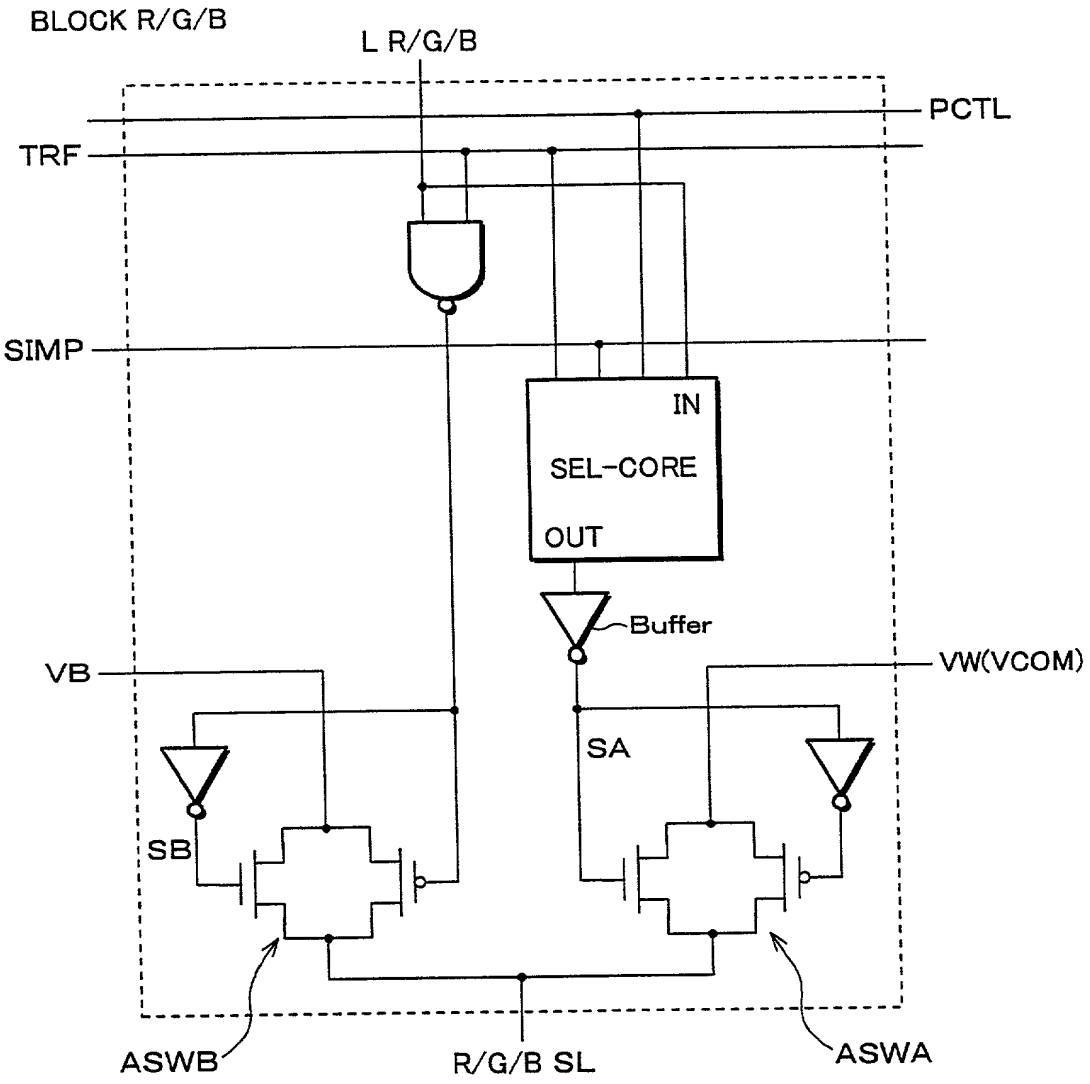

BLOCK R/G/B
L R/G/B
PCTL
TRF
SIMP
IN
SEL-CORE
OUT
Buffer
VB
VW(VCOM)
SA
SB
ASWB
R/G/B SL
ASWA

FIG. 127

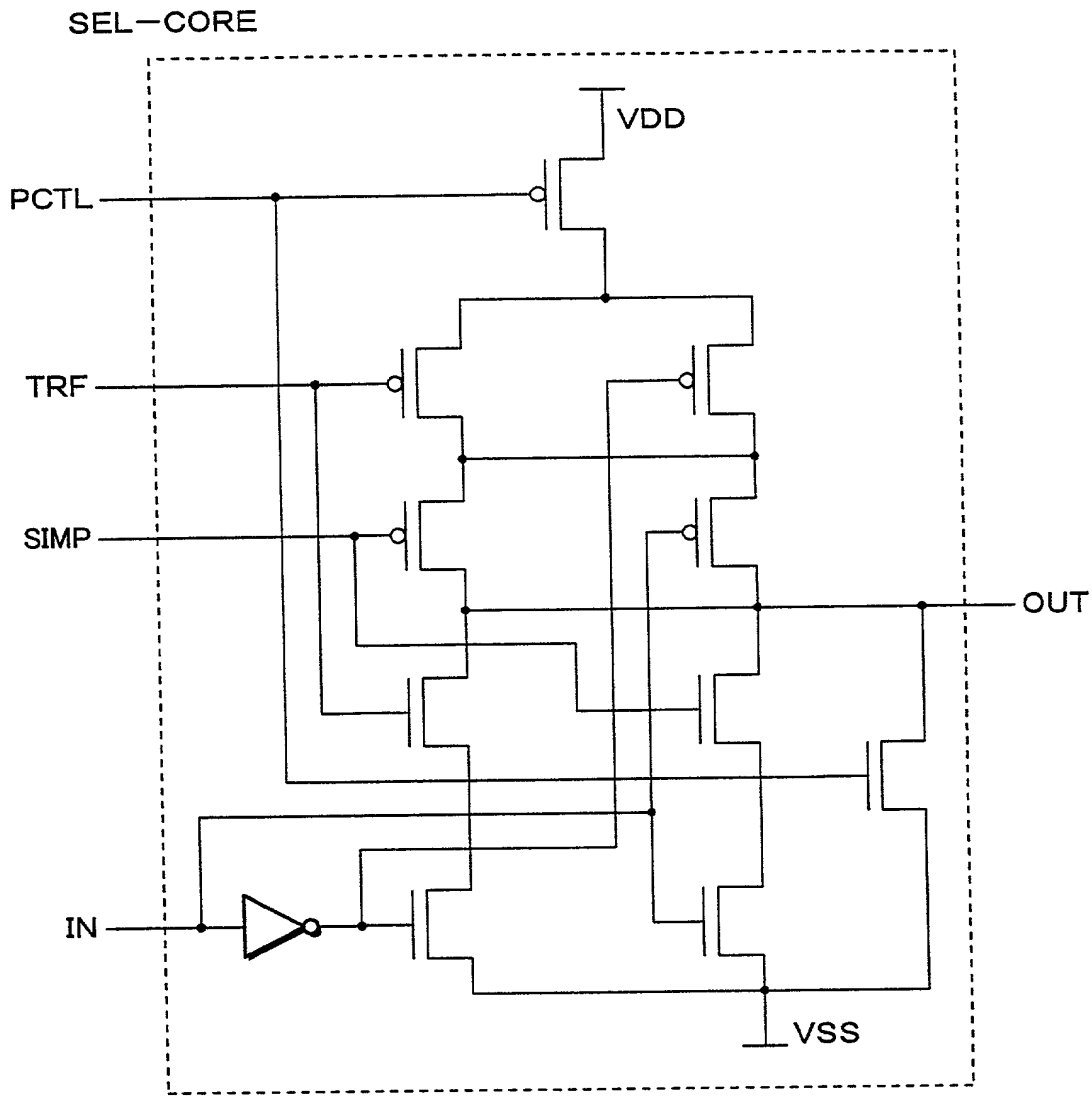


FIG. 128

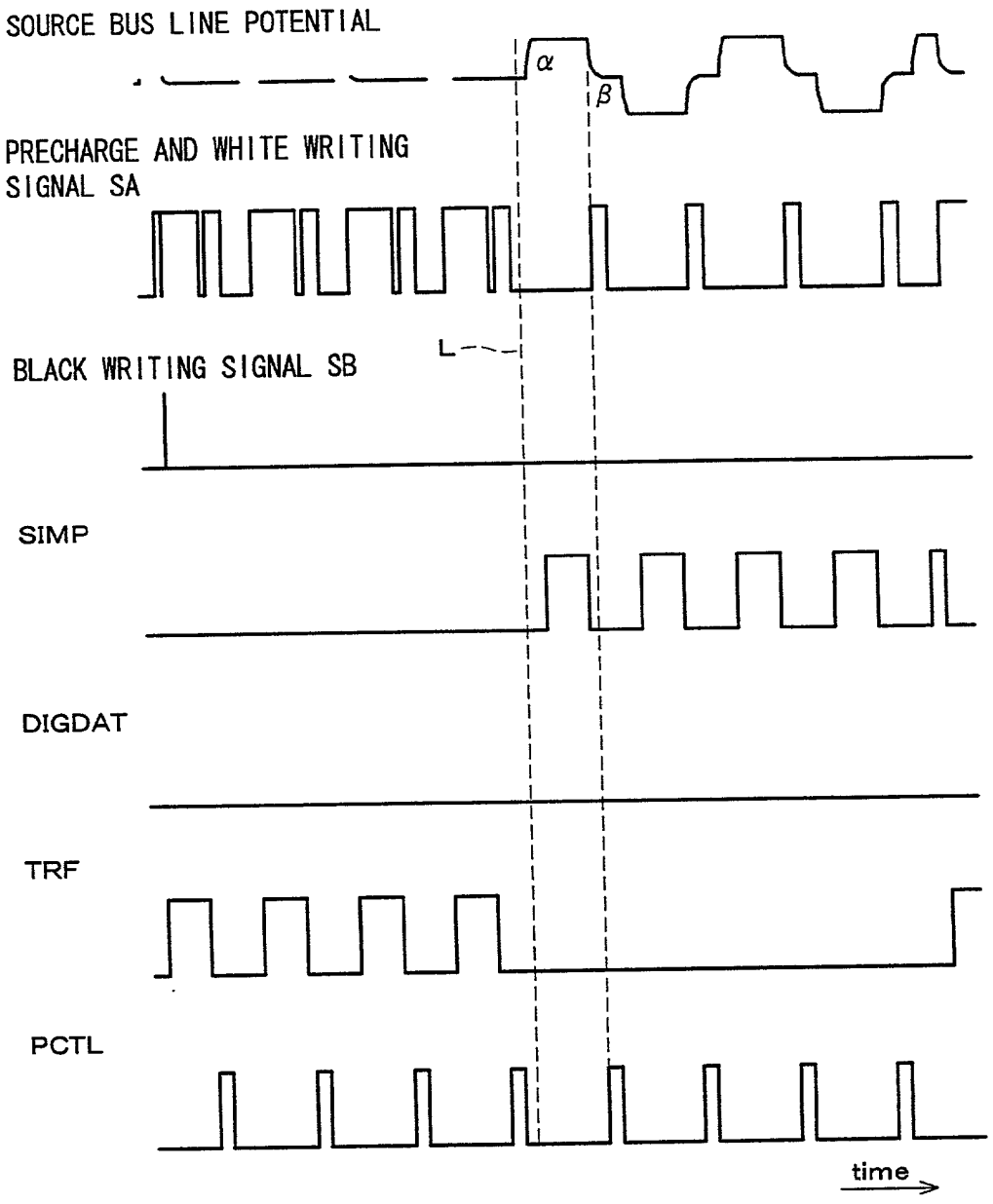

SOURCE BUS LINE POTENTIAL
α
β
PRECHARGE AND WHITE WRITING SIGNAL SA
L
BLACK WRITING SIGNAL SB
SIMP
DIGDAT
TRF
PCTL
time

FIG. 129

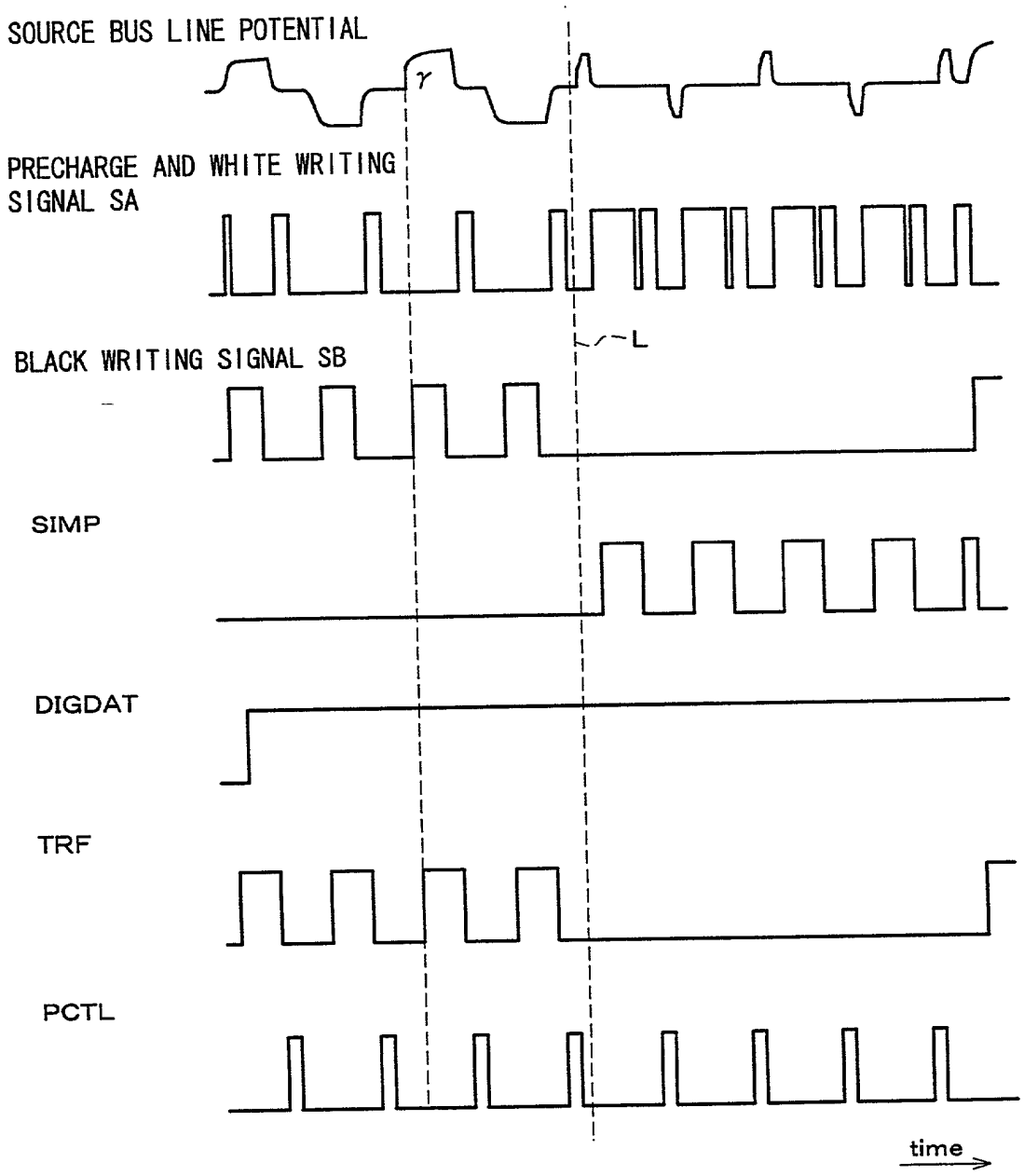

SOURCE BUS LINE POTENTIAL
PRECHARGE AND WHITE WRITING SIGNAL SA
BLACK WRITING SIGNAL SB
SIMP
DIGDAT
TRF
PCTL
time

FIG. 130

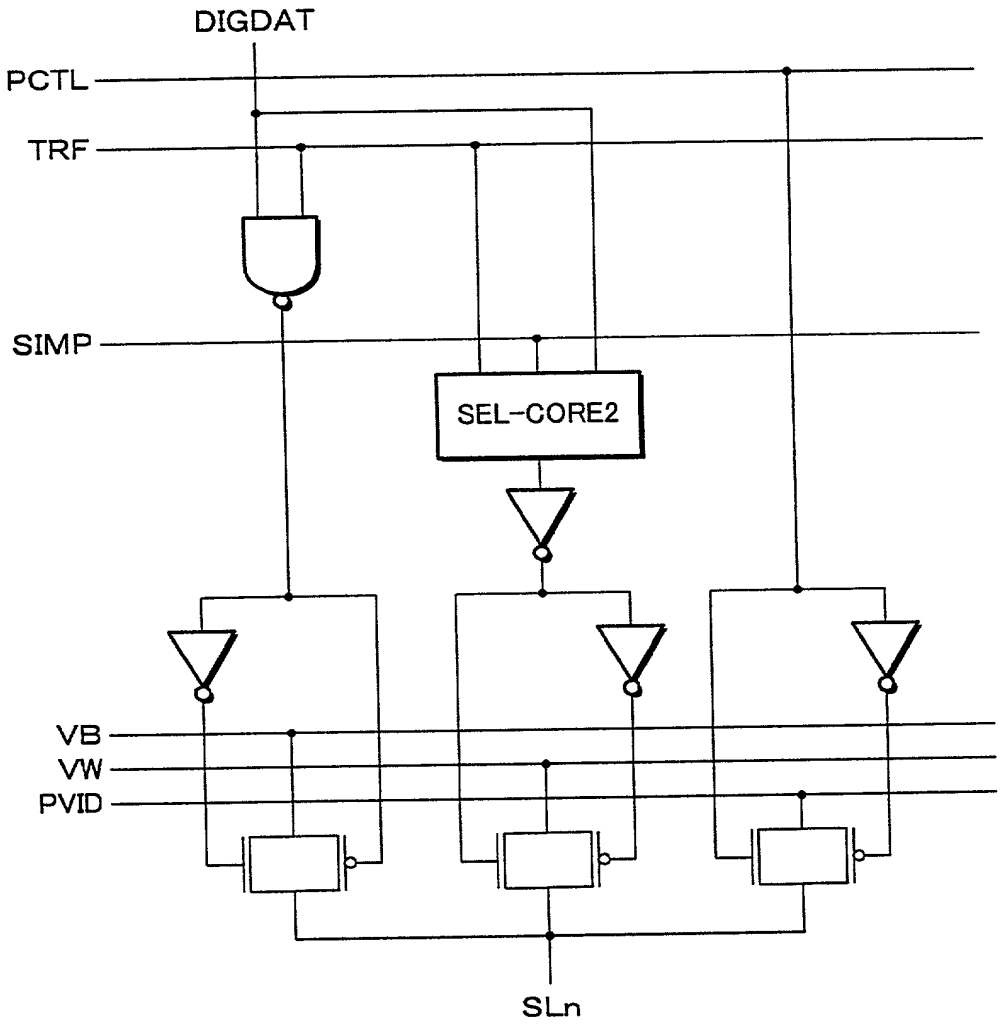
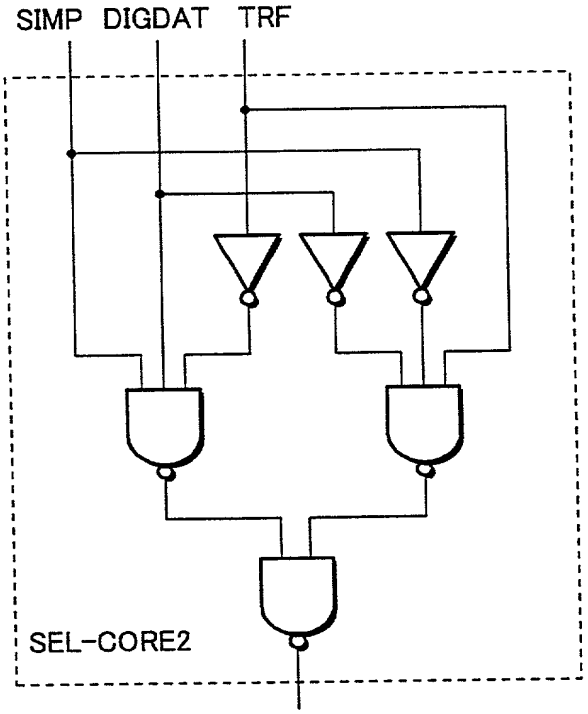


FIG. 131



EP 2 693 674 A1 20140205

JP2005050588A 20050224

FIG. 132

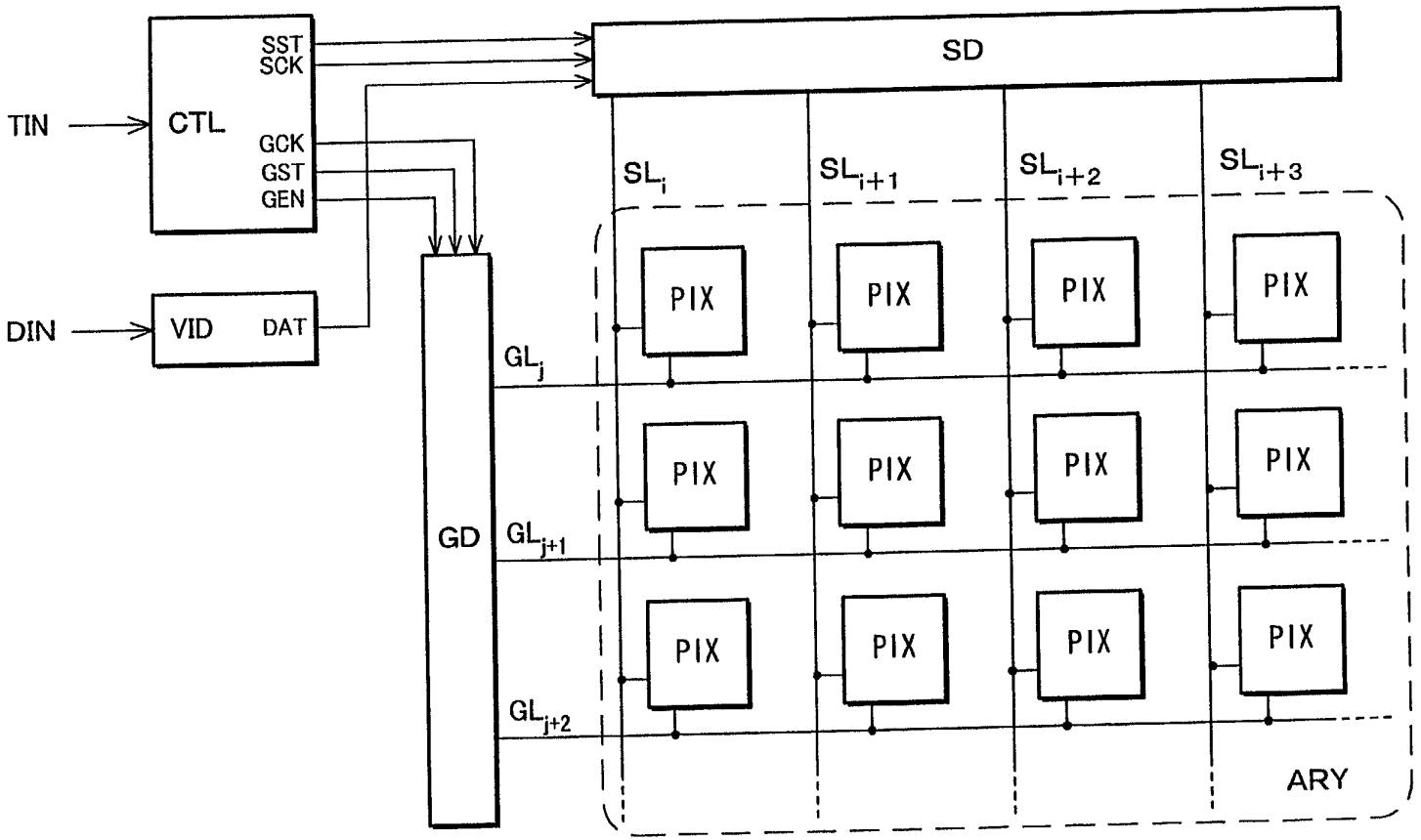


FIG. 133

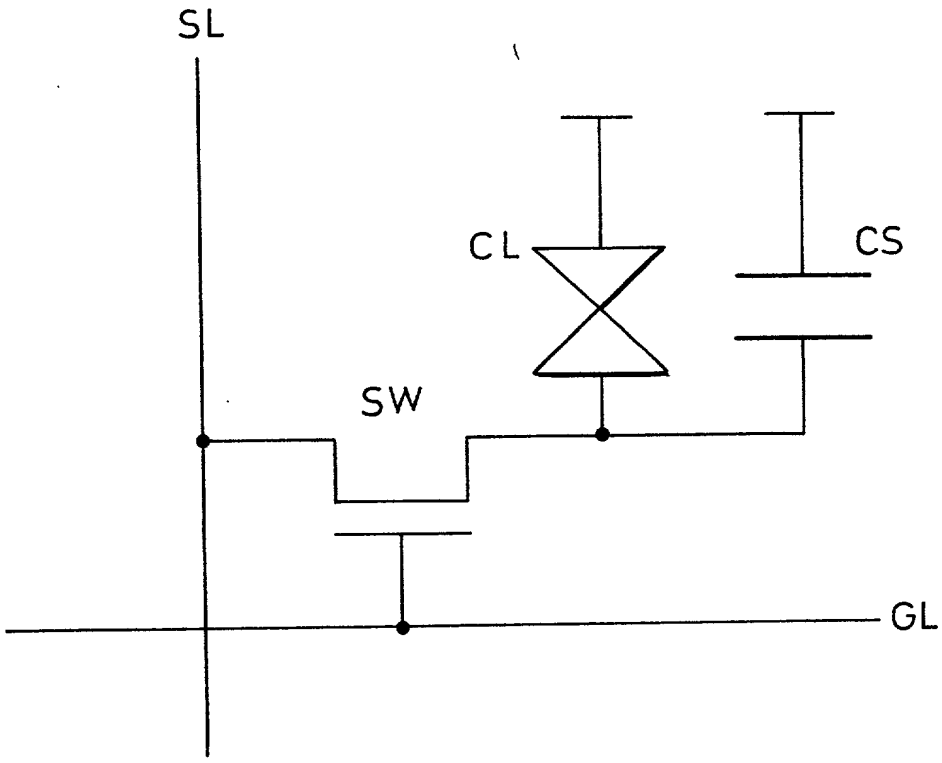


FIG. 134

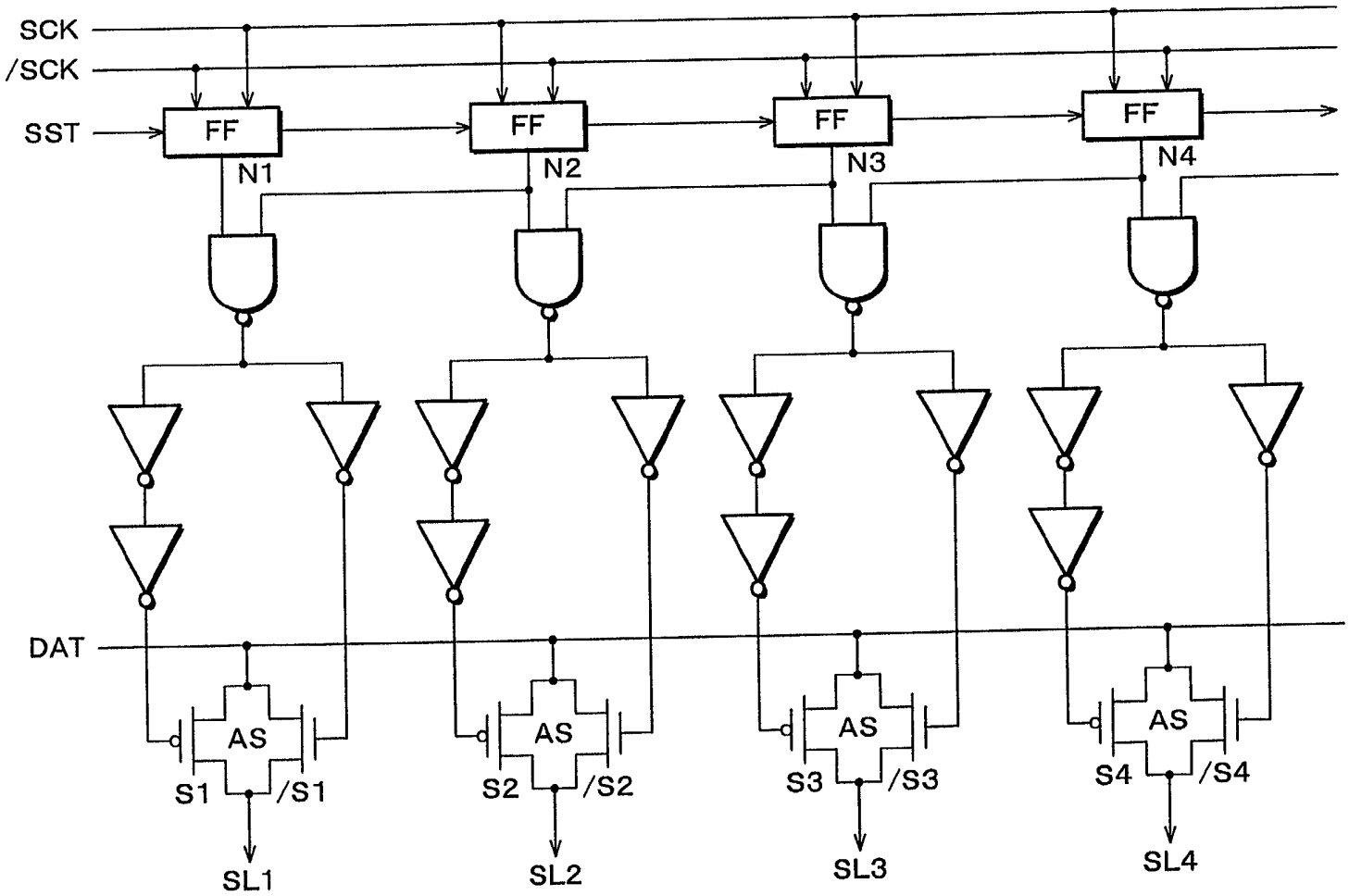

SCK
/SCK
SST
FF
FF
FF
FF
N1
N2
N3
N4
DAT
AS
AS
AS
AS
S1
/S1
S2
/S2
S3
/S3
S4
/S4
SL1
SL2
SL3
SL4

FIG. 135

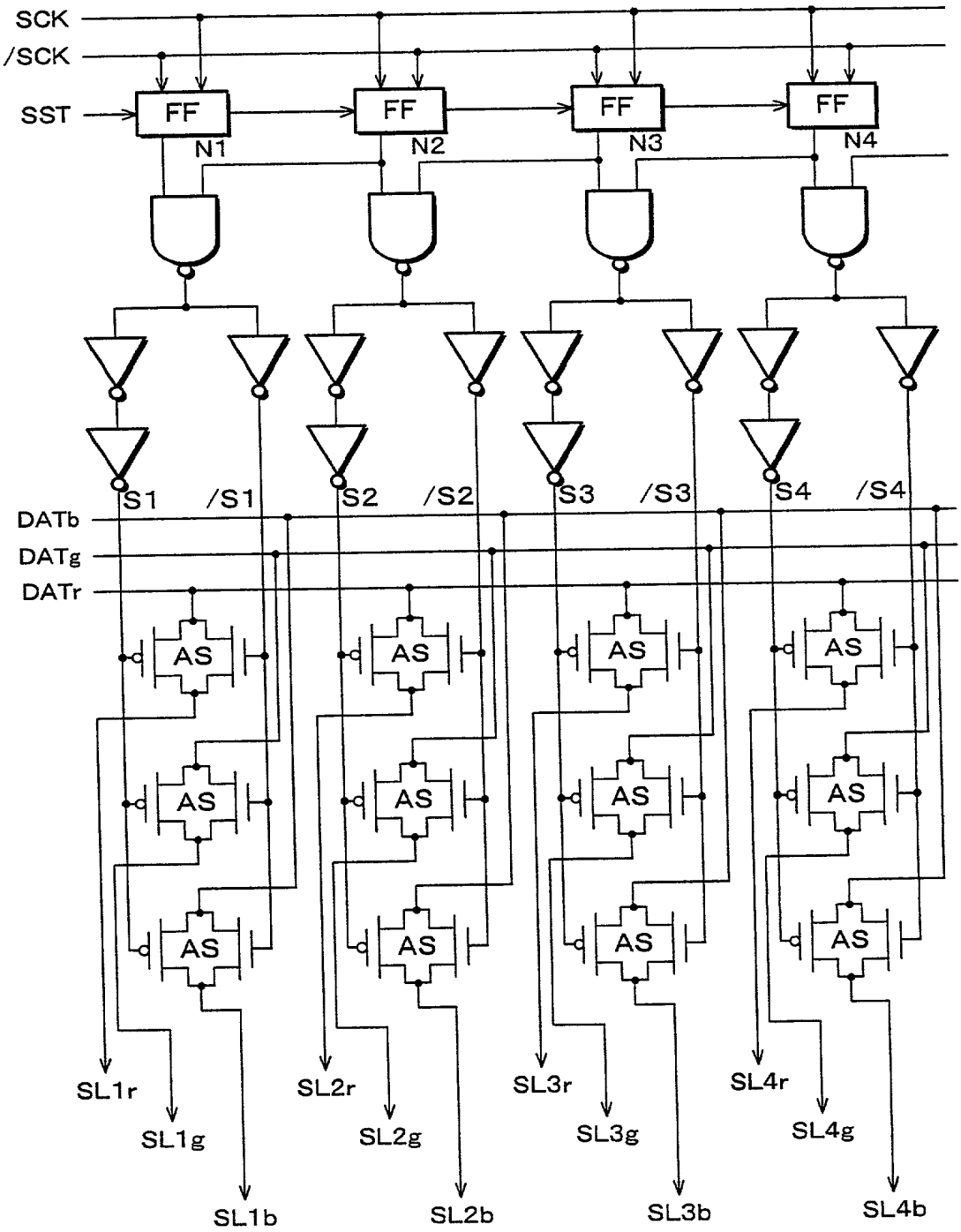

SCK
/SCK
SST
FF
N1
FF
N2
FF
N3
FF
N4
S1
/S1
S2
/S2
S3
/S3
S4
/S4
DATb
DATg
DATr
AS
SL1r
SL1g
SL1b
SL2r
SL2g
SL2b
SL3r
SL3g
SL3b
SL4r
SL4g
SL4b

FIG. 13B

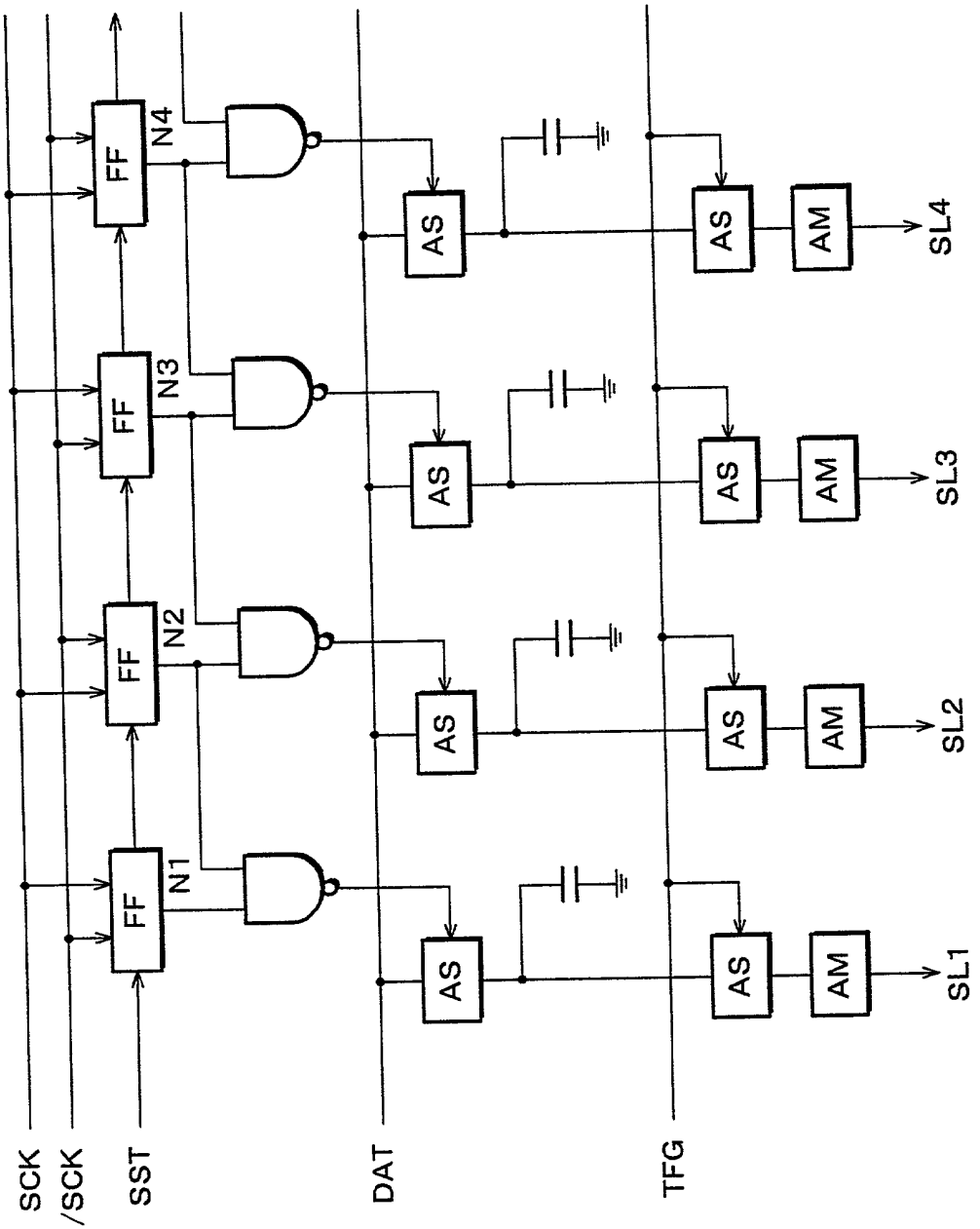


FIG. 137

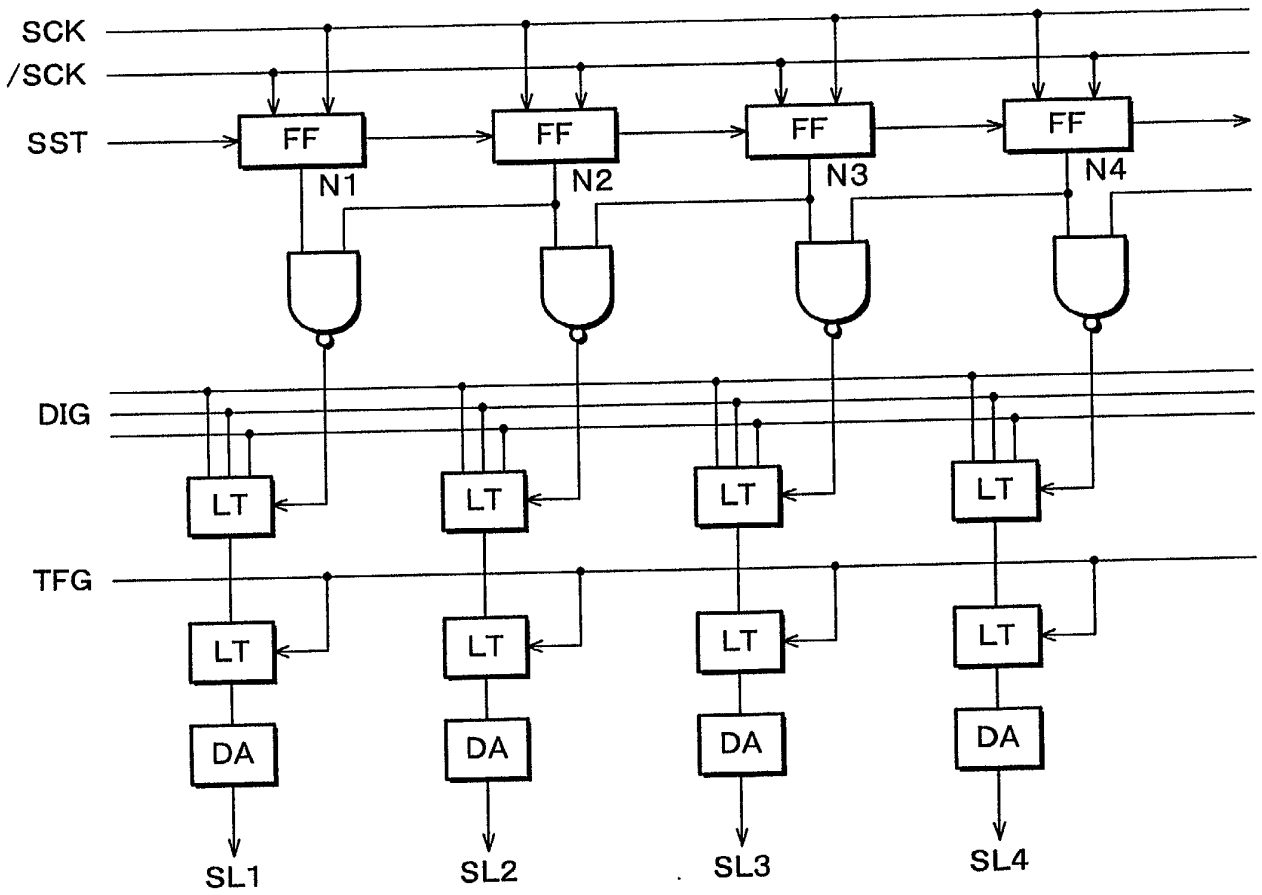

SCK
/SCK
SST
FF
FF
FF
FF
N1
N2
N3
N4
DIG
LT
LT
LT
LT
TFG
LT
LT
LT
LT
DA
DA
DA
DA
SL1
SL2
SL3
SL4

FIG. 138

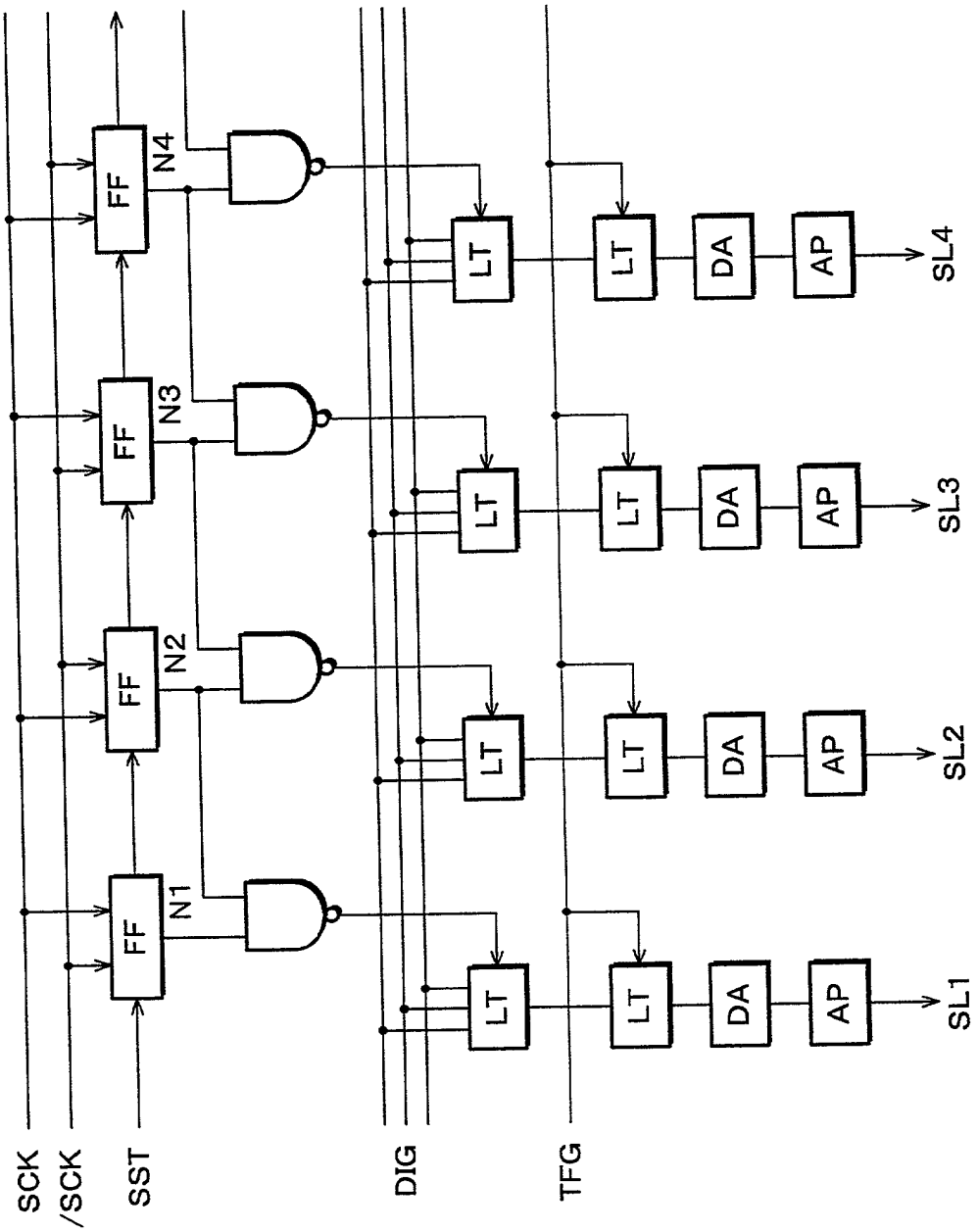


FIG. 13B

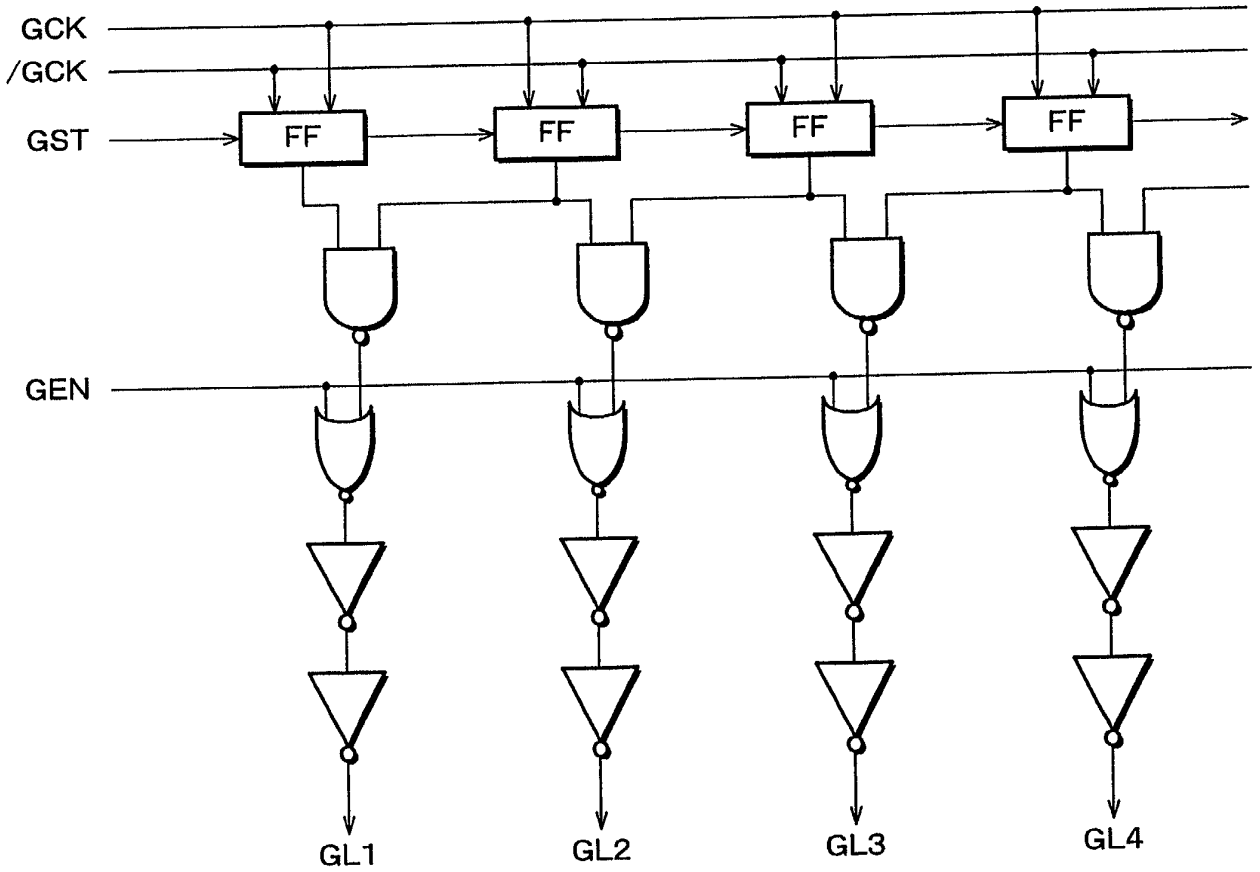


FIG. 140

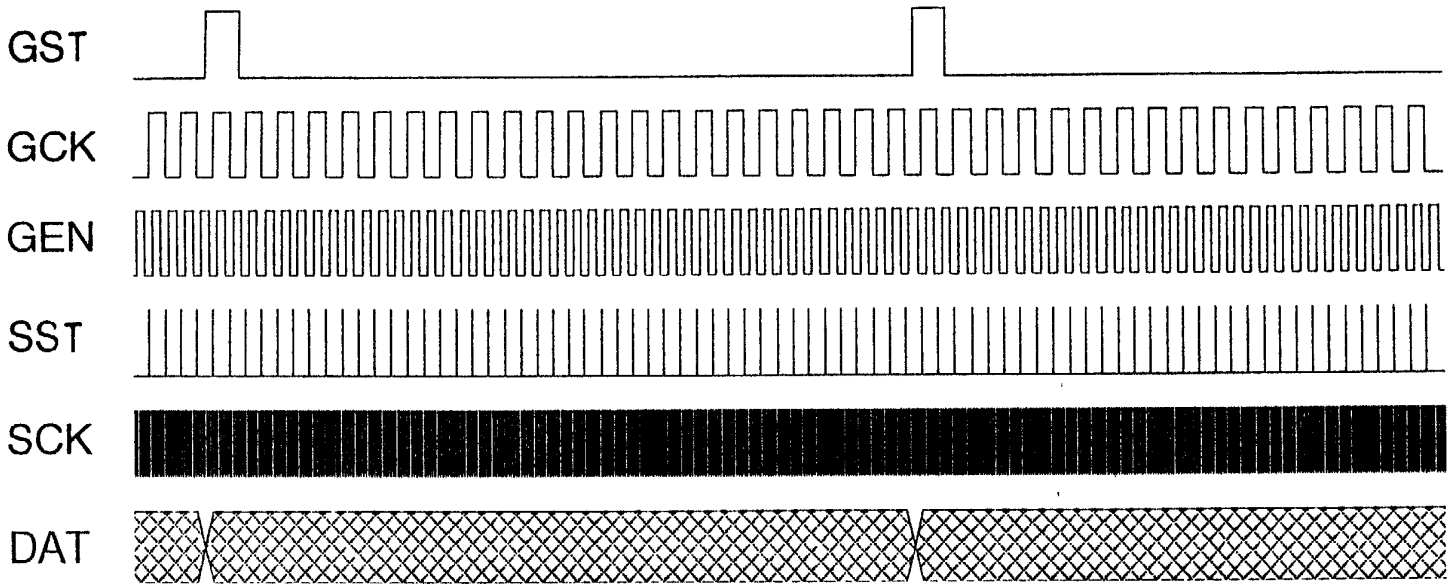
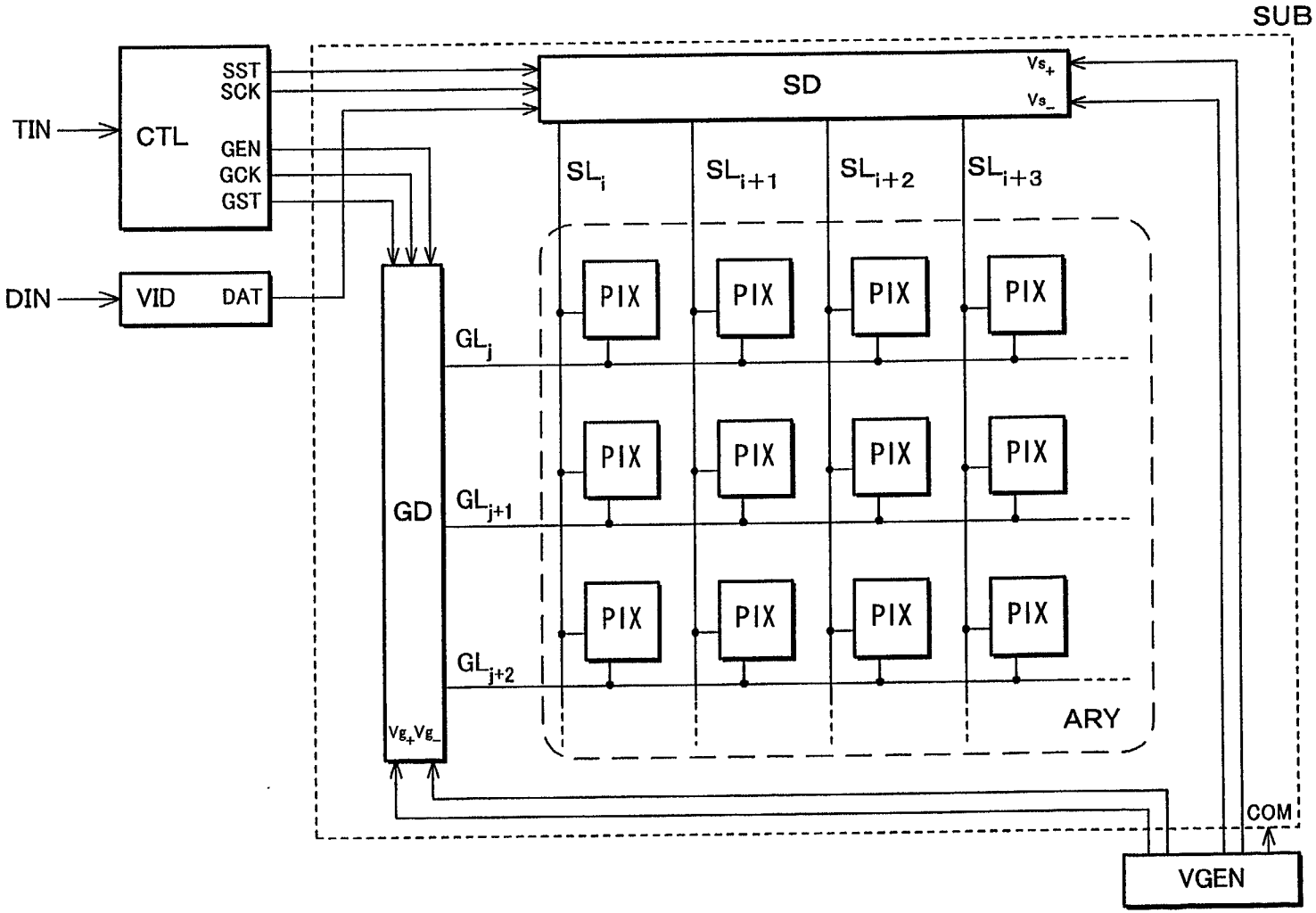


FIG. 1A1


SUB
TIN
CTL
SST
SCK
GEN
GCK
GST
DIN
VID
DAT
SD
Vs+
Vs-
SLi
SLi+1
SLi+2
SLi+3
GD
GLj
GLj+1
GLj+2
Vg+Vg-
PIX
ARY
COM
VGEN